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**Dissertation for the Degree of Doctor of Philosophy**

**Transformer-Based RF Power Amplifiers  
and Signal Generations in Silicon**

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**Graduate School**

**Dongguk University**

**2022**

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by


**Van-Son Trinh**

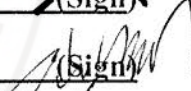
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Date of submission : 2022/06

Date of approval : 2022/07


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## **ACKNOWLEDGMENTS**

In the first place, I would like to express my profound gratitude to Professor Park Jung-Dong for his numerous encouragements, guidance, and support during my study and life at Dongguk University. Throughout the highs and lows of my Ph.D. journey, he has always been generous, attentive, available, and encouraging. Thanks to his extensive experience and firm and solid knowledge, I have learned the principles of RF integrated circuit design and gained valuable academic experience.

Also, I would like to thank all the committee members for their prudent and valuable guidance during my doctoral dissertation. It has been very helpful to have their constructive suggestions and opinions.

Taking this opportunity, I would like to thank all the people I have met and worked with at MEIC Lab. at Dongguk University, Dr. Don-Hwa Lee, Dr. Hyo-Hyun Nam, Jeong-Moon, Van-Viet, Young Joe, Hsiang-Nerng Chen, Tae-Wha, Hyeon-Seok, Jun-Hee, Van-Du, Hyeon-Hee, and Hyeong-Geun. I have taken a lot of technical help and instruction from my senior Hyo-Hyun. It is also a good chance to enrich knowledge and experience when working with other members. As an international student, it could be lonelier and more difficult for me to settle the life without the friendly help and the shares from other members and Vietnamese friends.

Most importantly, I wish to acknowledge and thank my family and my wife, Nguyen Thi Trang, for their endless support and love. It would not be possible for me to achieve what I have without their dedication and sacrifice.

## ABSTRACT

The last decade has witnessed a rapid growth of RF transceivers in various applications such as broadband wireless links for the 4<sup>th</sup> and 5<sup>th</sup> generations of communication, medical imaging, radar, and spectroscopy. Various performance merits are required for a transceiver platform specification, such as bandwidth, gain, linearity, efficiency, noise resistance, area occupancy, and power consumption. Modern transceiver design has faced challenges of deficiency in the output power with low efficiency for signal transmission due to the adverse effect of the scaling down of the MOS-transistor channel length to attain higher speed and lower power consumption in digital blocks. Moreover, the movement toward higher operating frequencies also degrades the intrinsic gain of active devices (i.e., MOSFET or BJT) and increases the loss of passive components (capacitors, inductors, transformers, and power combiners/splitters).

This dissertation deals with improving the power amplification and signal generation for RF transceivers in silicon. The first research topic focuses on enhancing efficiency and output power for power amplifiers in the various microwave and millimeter-wave regimes. The second topic deals with improving the harmonic rejection ratio in the frequency multiplier which is an essential building block in high-quality signal generation in the millimeter-wave regime. Regarding power amplification, we perform a detailed analysis of the impedance matching for push-pull amplifiers using a transformer-based matching circuit which is among the most frequently employed structure in CMOS power amplifier (PA) design. The reliability of the push-pull amplifiers has also been analyzed using network theory to ensure its stable operation when implementing matching components and biasing circuits to prevent common-mode oscillation. Several PAs designed with the established principles have been successfully demonstrated in X-band, E-band, and sub-terahertz (sub-THz) regions. To enhance the output power of the CMOS PAs, we have introduced a transformer-based novel power combiner operating with current and voltage modes at the X-band to boost the output power by higher than 25-dBm while achieving a power-added efficiency of 25-% in 65-nm CMOS. An

efficient power combining in the voltage domain at higher frequencies becomes more challenging due to the low self-resonant frequency (SRF) from the relatively lengthy routing structure of the transformer-based combiners at the millimeter-wave regime. To overcome this issue from the transformer-based power combining structure at high frequency, we have explored the potential usefulness of the high-way power combining architecture in the voltage mode and successfully demonstrated an E-band eight-way CMOS power amplifier in 65nm CMOS technology. The fabricated PA achieved up to 19-dBm of output power at 85-GHz which was the first E-band PA operating beyond the SRF of the transformer-based power combiner to date. As a core building block of the high-performance local oscillator (LO), frequency multipliers have been increasingly utilized in millimeter-wave LO blocks considering their wide tuning range and low phase noise performance. To further improve the harmonic rejection of the transformer-based push-pull doubler, we have introduced imbalanced capacitive loads to compensate for intrinsic impedance imbalance at the differential terminals of the transformers. The proposed methodology was applied an eight-time frequency multiplier operating at E-band in 65nm CMOS, and the prototype demonstrated more than 10 times of improvement in the harmonic rejection compared with that without the imbalanced capacitive loads.

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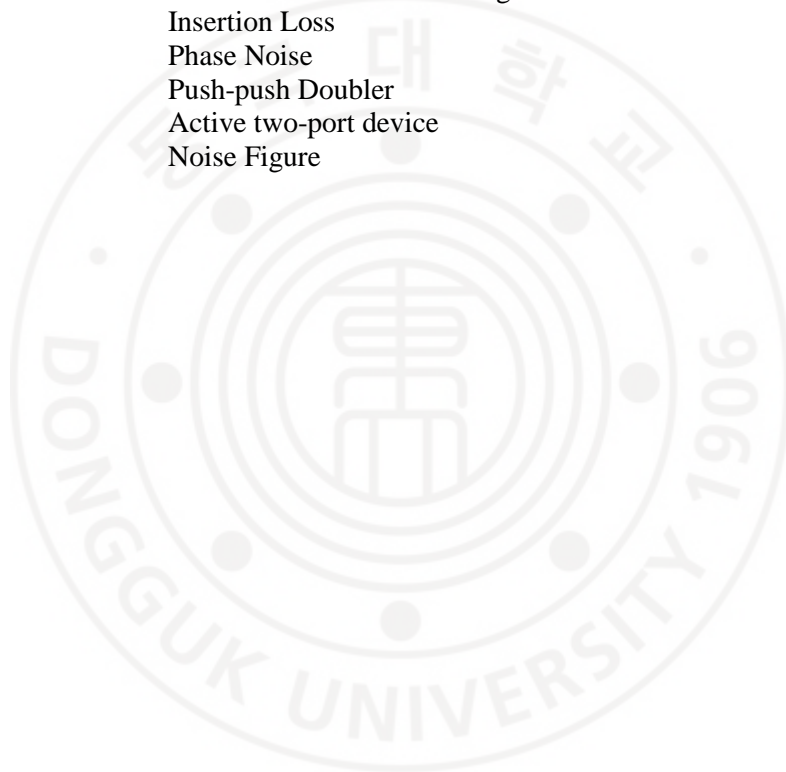
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## ABBREVIATIONS

IC	Integrated Circuit
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
PA	Power Amplifier
DA	Driving Amplifier
HPA	High Power Amplifier
TRx	Transceiver
Tx	Transmitter
Rx	Receiver
LO	Local Oscillator
IF	Intermediate Frequency
FM	Frequency Multiplier
HRR	Harmonic Rejection Ratio
CMOS	Complementary Metal-Oxide-Semiconductor
BJT	Bipolar-Junction-Transistor
HEMT	High Electron Mobility Transistor
FET	Field Effect Transistor
SOI	Silicon-on-Insulator
AESA	Active Electronically Scanned Array
LNA	Low Noise Amplifier
TRM	Transmitter/Receiver module
SPDT	Single Pole Double Throw
VCO	Voltage Control Oscillator
PLL	Phase Locked Loop
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
FMCW	Frequency-Modulated Continues-Wave
TF	Transformer
TF-based	Transformer-based
FoM	Figure-of-Merit
CS	Common Source
AC	Alternating Current
DC	Direct Current
CM	Common Mode
BEOL	Back End of Line
SRF	Self-Resonant Frequency
EM	Electromagnetic
HB	Harmonic Balance
CAD	Computer-Aided Design
RHP	Right-Half Plane
CCT	Current Combining Technique
VCT	Voltage Combining Technique
CPC	Current Power Combiner
VPC	Voltage Power Combiner

PCV	Power Combiner on Voltage domain
PC	Power Combiner
PS	Power Splitter
DAT	Distributed Active Transformer
UTM	Ultra-thick Metal
PAE	Power Added Efficiency
OP1dB	Output 1-dB gain compression point
Psat	Saturated Power
OIP3	Output Third Order Intercept Point
E2PN	Equivalent Two Port Network
ESD	Electrostatic Discharge
TMN	Transformer-based Matching Network
IL	Insertion Loss
PN	Phase Noise
PPD	Push-push Doubler
A2P	Active two-port device
NF	Noise Figure





# I. Introduction

## 1.1. Motivation

Transceiver, which has more than a century of development, still witnesses constant innovation to adapt to the rapid change of advanced integrated circuitry (IC) technologies and revenue itself with new physical characteristics found at higher frequencies. Specifically, recent advancements in IC technologies with increasing cut-off frequency allow transceiver systems to work at higher frequencies with the benefits of surging in operation bandwidth, ushering in the era of data explosion [1.1]. Ultra-low-power, low-cost transceivers also are becoming spot-light that adapt to connecting an increasing number of mobility devices in the “internet-of-thing” era, aiming to implement smarter systems [1.2]. Another trend of transceiver technology is the movement toward higher frequency with promising applications found at sub-terahertz such as secure scanning, and imaging in medicine [1.3]. The architecture of a transceiver might be varied for different applications and operating frequencies. However, most of them can be simplified with a radio-frequency (RF) interface shown in Figure 2.1.

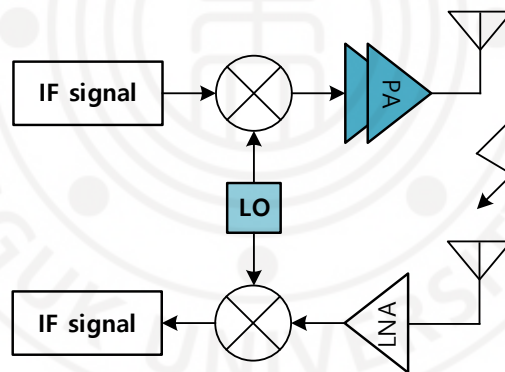


Figure 1.1. Typical simplified RF interface of a transceiver system.

In this thesis, we mainly focus on investigating and enhancing the performance of the power amplifier (PA) and the local oscillator in the transceiver architecture. Because power amplifiers are the most power-hunger block in a transceiver system, their efficiency dominates the energy efficiency of the TRx. The power efficiency is an especially critical factor for mobile devices to extend their battery usage time, which is one of the most important commercial user-performance. In addition, power amplifiers are the block working at the largest signal. Its linearity directly affects the spectrum efficiency of a TRx

system as surveyed in [1.4]. Also working in the large signal mode, the LO was required to provide clean and stable oscillation for the mixer to perform the conversion function between intermediate frequency (IF) and RF signals. Specifically, these criteria are quantified by the harmonic rejection ratio (HRR) for a frequency multiplier (FM), the flatness of output power over the sweeping frequency, and the phase noise of the input signal for the FM, which finally turns into the phase noise at the output with an increase of the multiplication factor.

The trends toward high-data-rate, ubiquitous wireless communication have opened up challenges and also opportunities for RF designers to implement high-efficiency power amplifiers on the advanced IC technologies. The recent development on physics-level platforms allows IC processes to achieve increasing cut-off frequencies ( $f_i$ ), but with lower supported supply voltage, and break down voltages as well. Table 1.1 shows the reducing trend of nominal supplying voltage for different technology nodes over the years. The reduced switching time benefits digital designs with smaller, faster, and lower-power designs. It also allows the RF interface to operate at a higher frequency. However, the less gain of the active device and the more severe loss of the passive components at high frequencies are hindrance factors to arrive at ideal high-efficiency, high-power, wide bandwidth, and high linearity PA designs. Similarly, there are also technical trade-offs between high-power, wide bandwidth, and low phase noise performances for LO implementation. Depending on the specification of the TRx system, a designer could determine which performances are of higher priority for a specific design.

Table 1.1 Characteristics of different technology nodes [1.5]

Production year	Technology node	Technology type	VDD (V)
1999	180	Bulk	1.8
2001	130	Bulk	1.2
2004	90	Bulk	1.1
2007	65	Bulk	1.1
2008	45	High-k	1.1
2010	32	High-k	0.97
2012	20	Multi-Gate	0.9
2013	16	Multi-Gate	0.86
2013	14	Multi-Gate	0.86
2015	10	Multi-Gate	0.83
2017	7	Multi-Gate	0.8

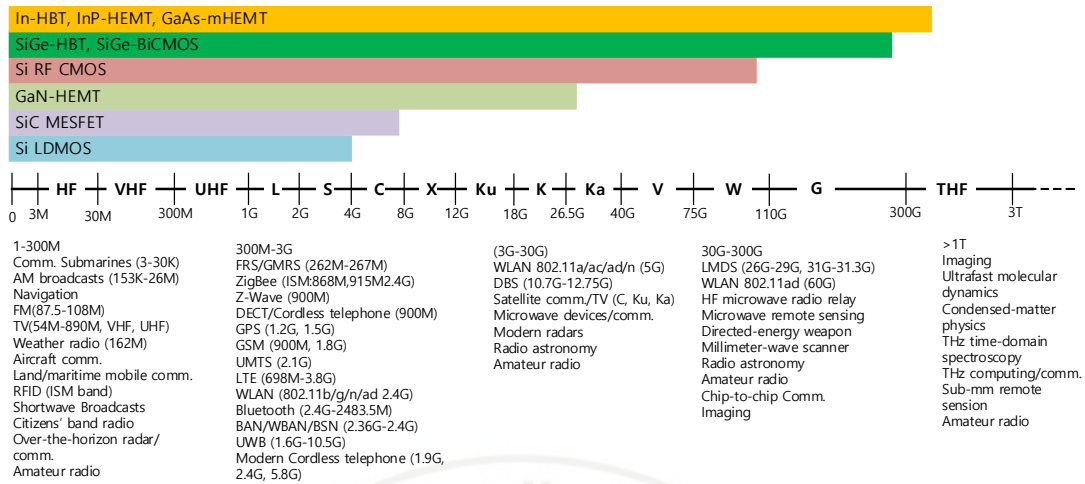


Figure 1.2. Applications of power amplifiers over frequency bands [1.4].

The graph of the application of power amplifiers distributed over frequency is illustrated in Figure 1.2 [1.4]. It also shows the typical technologies used at different frequencies. It is noticed that compared to the raw figure in [1.4], we have updated the frequency range of GaN-HEMT, Si RF-CMOS, and SiGe-BiCMOS based on our experiences with these technologies. It can be seen that power amplifiers (or transceivers in more general) have been found in various applications both civil and military. In this thesis, we have developed PAs, LOs and down-converter in X-band (8-12G), E-band (71-86G), and sub-terahertz band (280-GHz). Various applications can be found in these bands as listed in Figure 1.2. Herein, we briefly describe some applications at these bands in the followed sections including Active Electronically Scanned Array (AESA) radar at X-band, automotive radar at 77-GHz, wireless point-to-point communication in E-band, and wireless communication at the sub-terahertz band.

## 1.2. Applications

### 1.2.1. Active Electronically Scanned Array (AESA) in X-band

The basic concept of an AESA system is based on the fundamental working principle of a normal radar in which a transmitter (Tx) will send a short signal pulse through the antenna. Right after that, the antenna is disconnected from Tx to connect to an Rx by using a switch. By measuring the delay time of the returned signal, we can determine the distance to the reflecting object. In AESA systems, the signal from a single source (called the main station) is connected to an array of TRx modules that can control the phase of the signal on

each path separately (Figure 1.3). In this way, the beam can be steered quickly, thus AESA radar can scan the space much faster than using mechanical systems. Moreover, since sub-beams can be produced at different frequencies, the AESA radar can track a large number of targets simultaneously.

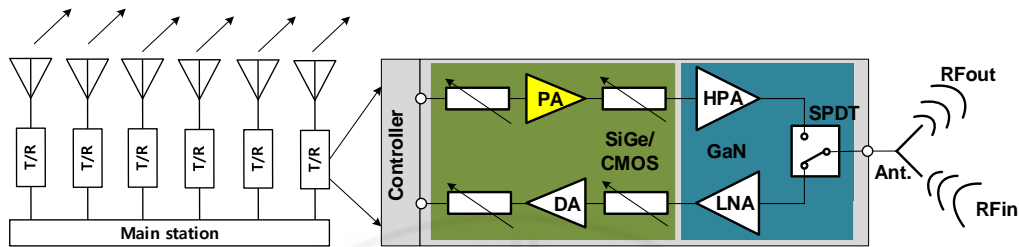


Figure 1.3. Simplified block diagram of AESA system.

Figure 1.3 also illustrates a block diagram of recent T/R modules (TRM) used in AESA systems. Typically, the TRMs consist of a front-end module that is connected to the antenna and a back-end module that is connected to the main station. The front-end block is typically implemented on GaN technologies. Due to the very high  $g_m$  of these technologies, we could design very high-power PAs (in the range of 46 dBm [1.6]). The LNA and the switch using GaN also can achieve very good performance. One disadvantage of GaN technologies has lied in their low integration level. Therefore, the back-end module with phase controllability is typically designed in SiGe or CMOS processes. To compensate for the loss of the passive phase delay blocks, it still requires a driving amplifier and power amplifiers in the back-end module, which is normally required to provide up to >20-dBm output power at the transmitting path to sufficiently drive the front-end HPA.

### 1.2.2 Automotive radar at 77-GHz

W-band is suitable for radar sensors in traffic vehicles because by using such a small wavelength, the radar could detect efficient small objects the size of a human, small cars, or traffic poles on the street. The high-frequency usage also makes the radar system faster in measuring high moving objects. In addition, W-band has stronger penetration property compared to a lower frequency, which makes it more reliable to be used in extreme environments such as bad weather conditions [1.7-1.8]. Due to these reasons, it is recommended by ITU for the automotive radar application (76-81 GHz) [1.9]. In [1.9], detailed specifications for automotive radars at different positions on a car are recommended.

Notably, the recommended output power of 10-dBm for the power amplifier is quite relaxed for RF CMOS processes which can cover the typical detection range of ~250m.

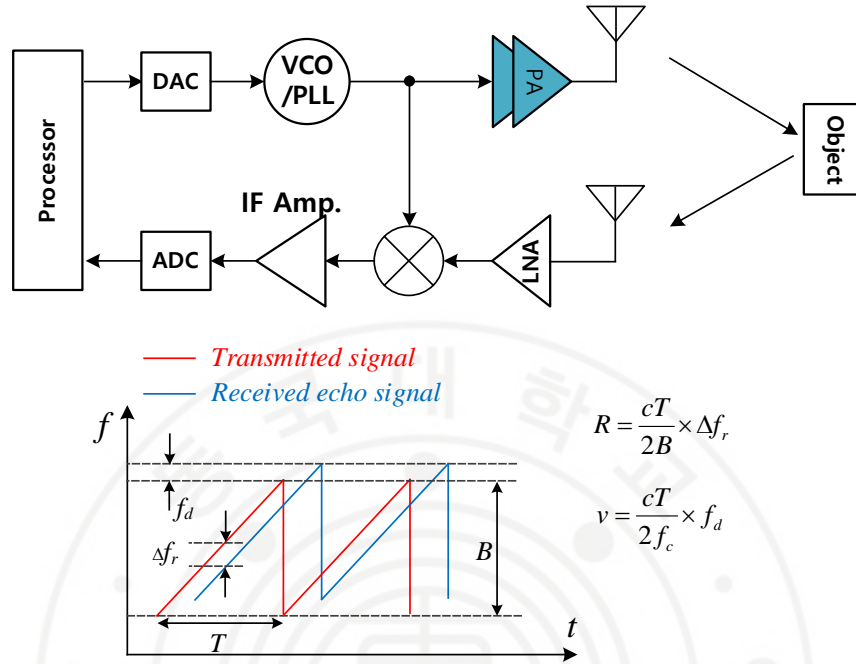


Figure 1.4. Simplified block diagram and working principle of an FMCW radar.

Automotive radars work based on the principle of the well-known frequency-modulated continues-wave (FMCW) radar which radiates continuous transmission power with the changed radiation frequency to detect the distance and velocity of the measured object. A simplified block diagram of a typical FMCW radar is shown in Figure 1.4. A detailed description of an FMCW radar can be found in [1.10]. An FMCW radar consists of a frequency synthesizer that can alter its output frequency signal based on the controlled signal from the processor. A transmitter including a PA and an antenna will radiate the frequency-modulated signal. A receiver using the same oscillation from the frequency synthesizer is used to detect the reflected signal. To detect the distance of the measured object, the FMCW radar measures the time delay of the reflected signal from the object to calculate the distance which is finally simplified to be the formula shown in Figure 4.1. Meanwhile, the velocity is measured based on the Doppler effects. On the basic, the frequency of the reflected signal is shifted up or down based on the relative velocity of the object with respect to the radar. By measuring the amount of the frequency shift, we could calculate the velocity of the

measured object. The equation to calculate the relative velocity of the object is presented in Figure 1.4 as well.

### 1.2.3 Point-to-point wireless communication in E-band for 5G backhaul

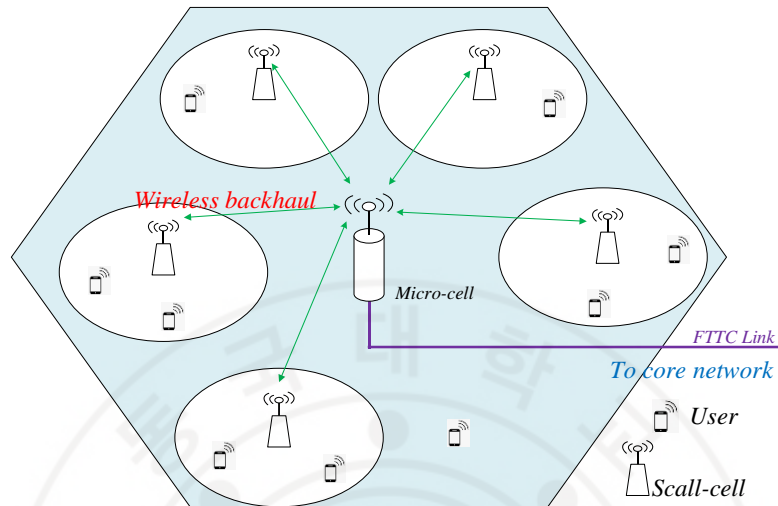


Figure 1.5. The logical architecture of the 5G backhaul network [1.11].

We are living in an era of data explosion generated by a huge number of connected devices which target building up a smarter life. This naturally leads to the born of the next generation networks (5G). The logical architecture of the 5G network is shown in Figure 1.5 [1.11]. A network's backhaul is the connection between the core network and its subnetworks. Through backhaul, the mobile network is connected to the wired network in 5G. Hence, 5G backhaul refers to signals between 5G cores and remote sites or networks. From the core network, 5G backhaul will need to support hundreds of gigabits of traffic per second. It is critical to the success of 5G to build out the backhaul infrastructure to allow for high speeds, large capacities, and wide bandwidths for multiple connected devices.

In the current infrastructure, fibers and wires are typically buried underground, or wireless antennas are attached to street lamps. Backhaul for generations before 5G will not be able to cope with the high density, low latency, and ultra-data-rate demands of 5G. A new backhaul infrastructure is therefore required. Backhaul over fiber generally proves to be difficult to deploy and expensive to install. Furthermore, laying enough fiber to connect everything to the core can take months. By eliminating wires or cables for wireless data transport, wireless backhaul facilitates easier installation. Backhaul via wireless (microwave and millimeter-wave) appears to be more readily available and easier to deploy. E-band (71-



86G) transceivers are a promising solution for 5G backhaul wireless links due to their supportability of wideband implementation ( $\sim 10\text{G}$ ). Moreover, transceivers at E-band could benefit from the reduced-cost and high-integrated level when Eband PAs are possible to be implemented in the CMOS process with sufficient output power of  $\sim 15\text{ dBm}$  to cover the typical required communication range of  $\sim 1\text{-}2\text{ Km}$  in urban areas [1.12-1.13].

#### 1.2.4 Wireless communication at the sub-terahertz band

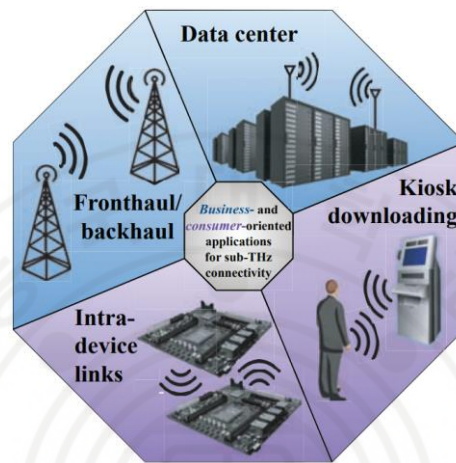


Figure 1.6. Target applications of wireless communication at sub-THz bands [1.17].

As shown in Figure 1.2, sub-terahertz (sub-THz) and beyond could be applicable in sensing and short-range wireless communication. Operating at shorter wavelengths could help an imaging system achieve better resolutions. The special absorption spectral of some materials and products to the sub-THz and THz bands also make spectroscopies at these bands to be employed in agriculture and food products, detection of concealed or dangerous objects, cancer scanning, etc [1.14-1.16]. Particularly, by shifting to sub-THz frequencies, wireless systems could potentially achieve a much broader bandwidth which is expected up to hundreds of Gbps.

The development of a 5G mobile network at microwave and mm-wave is currently almost complete. Venders are testing their system at the user level before it can be deployed on a large scale. Recent demonstrations of sub-terahertz transceivers have opened up a vision for a 6G network that could achieve an explosion in data rate, and time delay compared to a 5G network. The first standardization efforts for sub-terahertz band wireless connection could be found in [1.17]. Such short-range wireless links could be used in data



centers, device-to-device connections, front-haul and back-haul mobile networks, or Kiosk downloading as shown in Figure 1.6.

### 1.3. Thesis organization

In this thesis, we investigate design techniques to attain high-performance and robust push-pull power amplifiers. Based on that, we demonstrate power amplifier designs at X-band and E-band with the oriented performance of high-power, high-efficiency, and area minimization. An E-band frequency multiplier is also presented using transformer-based push-push doubler for a highly-clean local oscillation source. In sub-terahertz band, we present an implemented amplifier and a wideband receiver at 280-GHz in 130-nm SiGe.

Chapter 2 presents an analysis of the impedance matching network using transformers that are verified by measurement data for the transformer model as well as the synthesized matching formula. Besides the importance of impedance matching in improving the efficiency of the TF-based PAs, their robust operation against possible common mode oscillations is investigated, resulting in several useful guidelines to suppress instabilities.

Chapter 3 demonstrates three X-band power amplifiers with enhancement on either output power, operation bandwidth, or efficiency. First, we present a CMOS PA design on 65-nm CMOS utilizing a 6-way TF-based power combiner/splitter to achieve a well-balanced performance with an outstanding figure-of-merit (FoM) of 85-dB compared to other CMOS PAs. The second X-band PA on 65-nm CMOS was designed aiming at wideband operation and high output power. The third PA design is the demonstration of a proposed structure, called a “single-pull” amplifier which could be suitable for low-cost implementation.

In chapter 4, three PAs at E-band using push-pull amplifying structure are presented. First, we present a compact, high efficient PA design at 77-GHz on 65-nm CMOS for automotive radar application. Secondly, we demonstrate the feasibility of using a high-way voltage combination to enhance output power at the E-band with an 8-way PA design fabricated on 65-nm CMOS which could achieve ~19 dBm of measured output power. The final content of this chapter describes an mm-wave push-pull power amplifier using a neutralization inductive feedback network which is proposed to obtain good trade-offs between PA’s performance merits.

In chapter 5, an eight-time frequency multiplier (FM) design at E-band was described. The FM used three stages of push-push frequency doublers that applied a new balancing

technique for the TF-baluns to improve the harmonic rejection ratio (HRR). Experimental results are presented in comparison with other reported frequency multipliers recently.

In chapter 6, we present an amplifier and a receiver front-end at 280-GHz on 130-nm SiGe technology. The measured results are shown in comparison to the simulation values.

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## II. Impedance matching and stability analysis for TF-based PA

### 2.1 Introduction

Today, radio frequency integrated circuits (RFICs) include transformers (TFs) that are widely used for various purposes, such as impedance matching, impedance transformation, and signal conversions between single-ended and differential at various frequencies. If they are used to transform impedance or balance signals, transformers should ensure maximum power transfer to the load. Ideally, the input and output of a TF should be conjugately matched to its source and load impedances. Designing an efficient transformer network has been considered an essential task which has been implemented with several iterations with the aid of computer simulation since the input and output impedance are simultaneously affected by each other owing to the reciprocal nature of a passive network.

In this chapter, we investigate on a TF-based impedance matching network utilizing a simplified two magnetically coupled coils model connected to a source and a load. We investigate the matching requirement at two ports depending on the transformer parameters as well as the source or the load impedance connected to its counterpart port, and a detailed analysis of various impedance conditions for the transformer network is presented. Based on this work, analytic formulae for constructing a transformer network with a resistive load having a parallel tuning capacitor are provided. We also examined on-chip transformers implemented in 0.18  $\mu\text{m}$  CMOS technology to assess the validity of the proposed work.

The prevalence of a differential amplifier in common-source (CS) configurations is owing to its distinct benefits. Table 2.1 presents a comparison between the TF-based pseudo differential amplifiers (also called push-pull amplifiers) and CS single-ended amplifiers. The differential pair combines the power of two active devices to a load, thereby helping to release the voltage stress on the device's drains. It is a well-balanced structure when implying the natural two-pole property of an AC signal which maximizes the combining efficiency, mitigates CM interference and noise, and facilitates circuit layout owing to the symmetry structure. Therefore, the differential pair is commonly used as the unit cell when output power combining is exploited for a higher output power. However, it is well known that a CM oscillation can be triggered in a differential amplifier at a high frequency if the losses in the path of any feedback loop are not significant enough to guarantee robust stability. This chapter also deals with issue of detecting instability and stabilizing the network in the early stages of the design.

Table 2.1. Comparison between TF-based pseudo differential amplifiers and common source single-ended amplifiers

	TF-based pseudo differential amplifiers	Common source single-ended amplifier
Output power	$Z_{out}=Z_{device}/2 \Rightarrow$ could support four time output power larger than CS amplifier with the same $Z_{out}$	$Z_{out}=Z_{device} \Rightarrow$ support no power combination
Neutralization	Can be neutralized by cross-connected capacitors between the gates and drains $\Rightarrow$ broadband and easy in layout	Typically uses de-Qing resistors in the gate or use RC-feedback between drain to gate $\Rightarrow$ trade-offs between stabilization and loss
Layout	More compact with TFs	Less compact (LC or Tline matching)
Instability issue	Suffer from common-mode instability $\Rightarrow$ can be easily suppressed by neutralizing capacitor and de-Qing feedback paths	Suffer from odd-mode instability when using common-mode power combination $\Rightarrow$ can be suppress with de-Qing odd-mode resistors
Efficiency	Get worse at high frequency due to the loss of TFs	Achieve better efficiency at high frequency with TLine-based matching networks
At $F > f_{max}/2$	Loss of TFs are significant compare to gain of transistor $\Rightarrow$ not suitable to be used	More suitable because LC or Tline matching offer less loss compared to TF-based matching

## 2.2 Impedance matching for transformers

The magnetic coupling between two or more conductors in a passive transformer allows an input signal or input power to be transmitted to the load. An example of an implemented on-chip 2:1 transformer on silicon is given in Figure 2.1. The series resistance of each winding is quite significant when winding TFs are fabricated on a silicon substrate. This is because the windings are fabricated on relatively thin metal layers within BEOL dielectric layers, and the skin effect plays a role in the series resistance. Transformers model typically consists of two magnetically coupled coils, as shown in Figure. 2.2. This simplified transformer model relies on five parameters: series resistance ( $R_1$  and  $R_2$ ), inductance ( $L_1$  and  $L_2$ ), and coupling coefficient, which indicates the amount of magnetic coupling between the two windings [2.1].

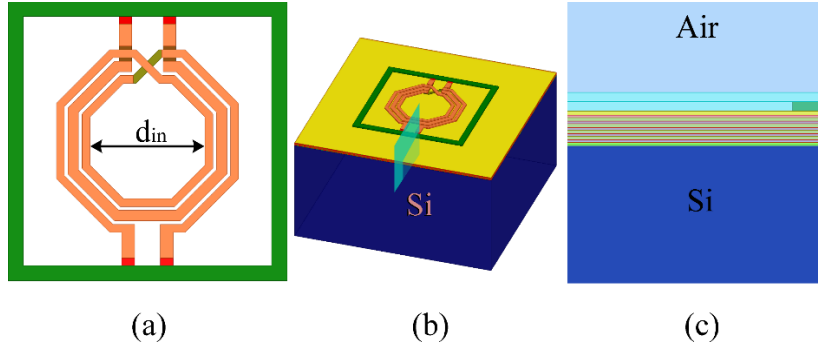


Figure 2.1. On-chip 2:1 TF structure for 3D electromagnetic simulation: (a) the front face, (b) a 3D view in HFSS, and (c) a side view of the layer stacks.

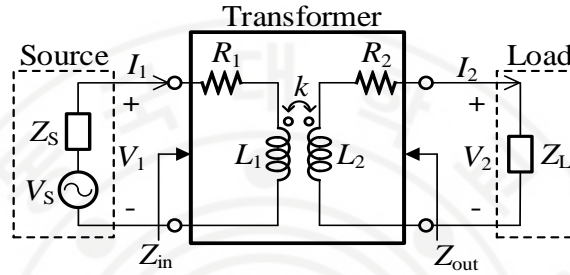


Figure 2.2. Magnetically coupled TF model with load and source.

It is defined that  $n=L_1/L_2$  is the turns ratio between the two wounds. Since the complexity of the model and analysis was considerably increased as a result of parasitic coupling capacitance, the effect was marginal at the frequency of interest (below SRF) when it was considered in this section. Following the basic low-frequency model, transformers are widely characterized as core circuits in many studies since the physical size of transformers tends to be considerably smaller than the guided wavelength at operating frequencies [2.1]. Due to this, it is possible to interpret dominant physical phenomena occurring in TFs at operating frequencies well below the transformer's SRF with inductors and magnetic couplings between them. The conjugate matching on both sides of the TF is either possible if the transformer is ideal ( $R_1=R_2=0$ ) or if  $Z_s$  and  $Z_L$  satisfy the conditions given by [2.2]

$$\begin{cases} X_L = -\omega L_2, X_S = -\omega L_1 & (2.1.1) \\ R_L = R_2 \sqrt{1+k^2 Q_1 Q_2}, R_S = R_1 \sqrt{1+k^2 Q_1 Q_2} \end{cases} \quad (2.1.2)$$

The maximum available gain of a transformer in the case of simultaneous conjugate matching conditions on both sides of the transformer given by [2.2] as



$$G_{T_{\max}} = 1 - 2 \frac{\sqrt{k^2 Q_1 Q_2 + 1} - 1}{k^2 Q_1 Q_2} \quad (2.2)$$

Even (2.1) provides the general solution for the load and the source of a transformer network, the more frequently used matching style for a transformer is to use parallel capacitors at their input and output as shown in Figure 2.3. This structure offers great convenience in layout, and any parasitic capacitances of the active devices the transformer is connected to are also easily aborted by the parallel matching capacitor. The optimum values of the resistance and capacitance in the parallel configuration were reported in [2.2] to be

$$\begin{cases} R_{L_{opt}} = R_2 \sqrt{1 + k^2 Q_1 Q_2} \left( 1 + \frac{Q_2^2}{1 + k^2 Q_1 Q_2} \right) \\ C_{topt} = \frac{L_2}{R_2^2 (1 + Q_2^2 + k^2 Q_1 Q_2)} \end{cases} \quad (2.3)$$

To verify the transformer model and the EM simulation in HFSS, we implemented and measured a single transformer in a 0.18  $\mu\text{m}$  CMOS process. Moreover, to demonstrate the validity of the parallel matching equation of (2.3), we fabricated a bunch of transformer networks in which only the parallel matching capacitor was varied. Photographs of the stand-alone transformer and its prototypes with different parallel matching capacitors fabricated on a 0.18  $\mu\text{m}$  CMOS process are shown in Figure 2.4

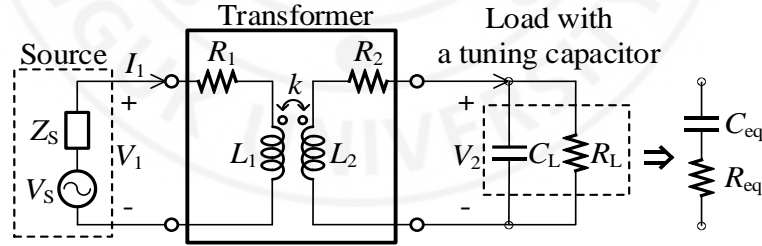


Figure 2.3. The TF impedance matching network using a parallel capacitor.



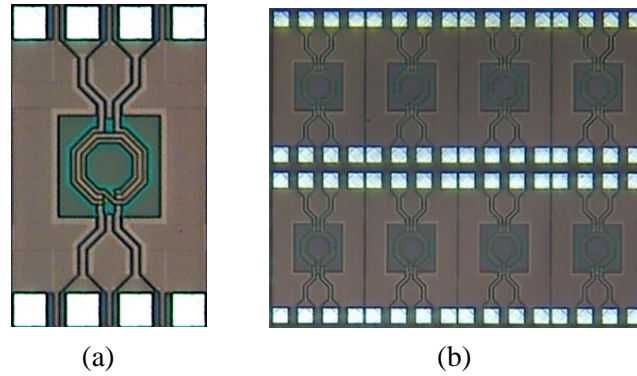


Figure 2.4. Photographs of the on-chip TFs in  $0.18 \mu\text{m}$  CMOS: (a) the standalone 2:1 transformer, and (b) transformers with parallel tuning capacitors.

From the measured s-parameters of the standalone 2:1 transformer, its parameters including resistances and inductances of the two coils and the coupling factor were extracted, which are shown in Figure 2.5 in comparison with its simulation results from the 3D model in HFSS. The extracted maximum available gain of the fabricated transformer was also shown in Figure 2.6 beside its counterpart on simulation. Overall, the simulation results corresponded well with the measured results. It can be seen that lower measured quality factors were recorded, which would be caused by several lossy factors which were not modeled in HFSS such as the roughness of the metal coils. Moreover, in the real case, loss tangents of dielectric materials can vary depending on the frequency, while in HFSS they are regarded as constants.

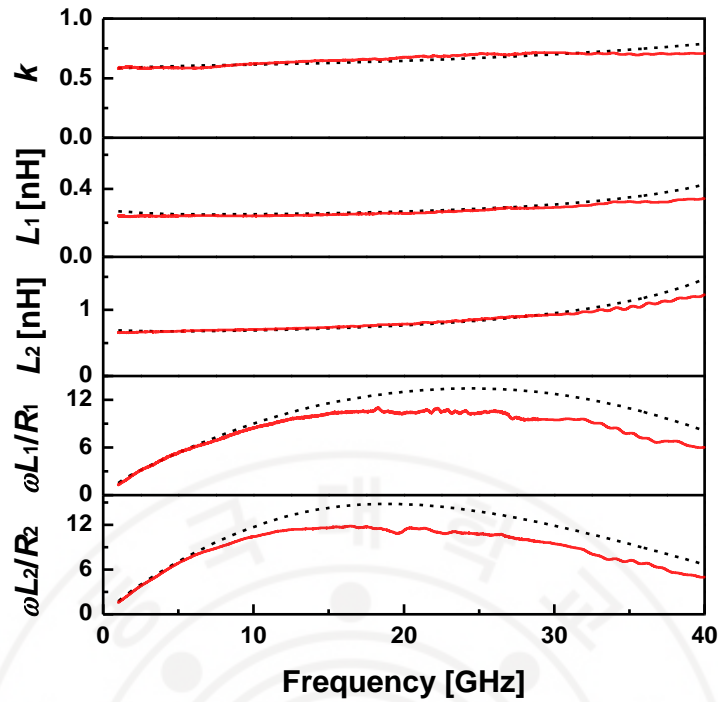


Figure 2.5. Effective parameters of the on-chip 2:1 TF on simulation (dashed line) and measurement (solid line).

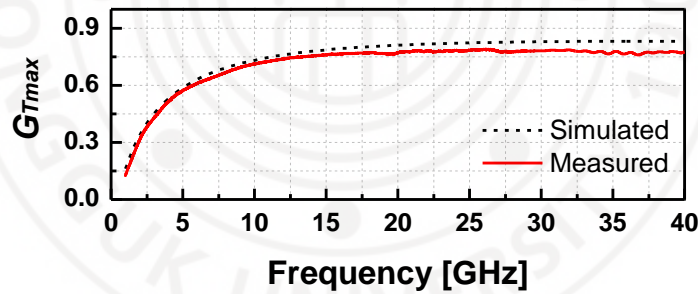


Figure 2.6.  $G_{Tmax}$  versus frequency of the on-chip 2:1 TF.

The matching equation of (2.3) was validated by measuring several fabricated transformers with different parallel capacitors at the load. We de-embedded the S-parameters from the RF pads and transmission lines. Afterward, power efficiencies for specific loads of  $50 \Omega$  and  $100 \Omega$  were obtained as shown in Figure 2.7. The data showed that the optimum  $C_l$  for both loads differed by about 20 fF (nearly 7%) from the simulation. This shift can be explained by the difference in  $C_{l,opt}$  between the model and the fabricated transformer based on the extracted parameters. This could also be a result of process variations resulting in a different nominal capacitance than what was specified by the manufacturer. The similarity

between the measured results and the calculated data from the formula (2.3) proves the helpfulness of the analytical equation.

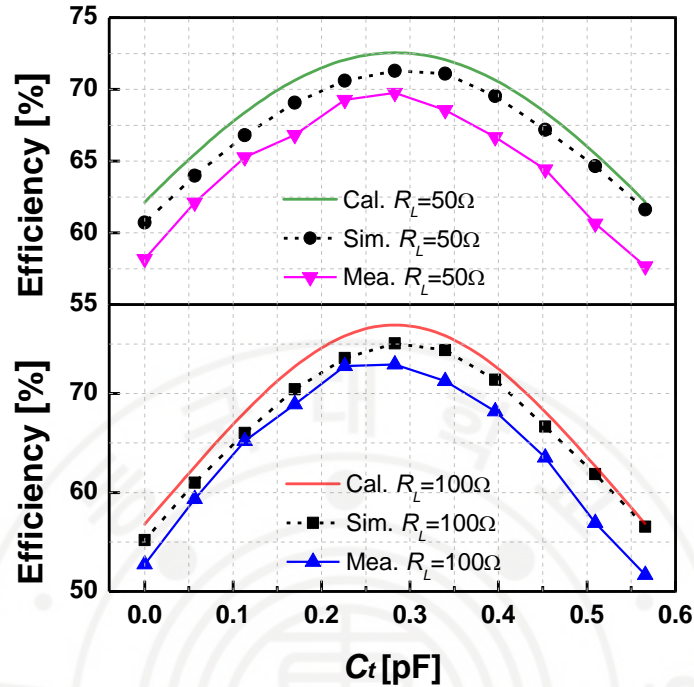


Figure 2.7. Power efficiency versus parallel tuning capacitances for the on-chip 2:1 TF at 10 GHz.

## 2.3 Common-mode instability in push-push power amplifiers

### 2.3.1 Introduction

The differential pairs of common-source (CS) transistors are commonly used as unit cells when output power combining is exploited for a higher output power [2.3]-[2.4]. During the early stages of the design process, it is crucial to detect instability and stabilize the network. Small-signal analysis has proven to be highly effective in identifying the major sources of instability in circuits with only a minimal computing effort required [2.5]-[2.6]. Despite this, there are still unstable points visible only at specific levels of RF input, and a small-signal analysis cannot detect them [2.7]. A transient simulation is an effective way to examine the unwanted behaviors of a circuit in the large-signal regime, but the computational resource requirements are high for complex designs [2.8]. To determine the stability of the circuit, designers should excite the circuit, such as by a step function in the supply and bias nodes. Harmonic balance simulations have also proven a promising way to detect instability, although the conventional HB simulator commonly found in CAD

programs has difficulty seeing it [2.7]. With additional applied methods, it can detect instabilities efficiently by using HB simulation [2.9], [2.10].

CAD tools can detect instability in a design. Still, it is quite a complex task since designers need to figure out the root cause of the instability to fix the design efficiently and achieve a good balance between stability and other performances. Manual analyses are important to thoroughly understand a specific circuit structure. The works in [2.11]–[2.12] had introduced some fundamental analysis on the stabilization of some circuit structures. One of the structures taken considerable interest from researchers in stability analysis is multi-branch paralleled PA because it uses power dividers and combiners between PA stages, which makes it prone to odd-mode instability. This issue has been investigated carefully both in the small-signal and large-signal domains in [2.5], [2.6], [2.10]. In [2.13], the authors have shown that a bypass capacitor connected to a non-ideal ground could lead to instability in push-pull amplifiers. In [2.14], we show that a differential amplifier can suffer from CM instability because of the gate inductance from the biasing line and the parasitic series coupling capacitance between the two coils of the input transformer.

### *2.3.2 Oscillation mechanism in differential amplifiers*

A pseudo-differential pair and a push-pull amplifier are widely used differential pair types in the microwave, with the output configuration demonstrated in Figure 2.8(a), and Figure 2.8(b), respectively. As the primary loss mechanism of CM signals, the inductive coils have relatively small parasitic series resistances, which makes the structure susceptible to instability. The combined effect of  $C_{gd}$  and the source's input impedance results in a positive feedback loop for the amplifier, leading to oscillations when a triggering signal is applied. Figure 2.8(c) shows a transient simulation of a differential push-pull PA implemented using 180-nm 1P6M CMOS technology. The amplifier oscillates when the supply voltage is turned on without an input signal, based on the simulation.

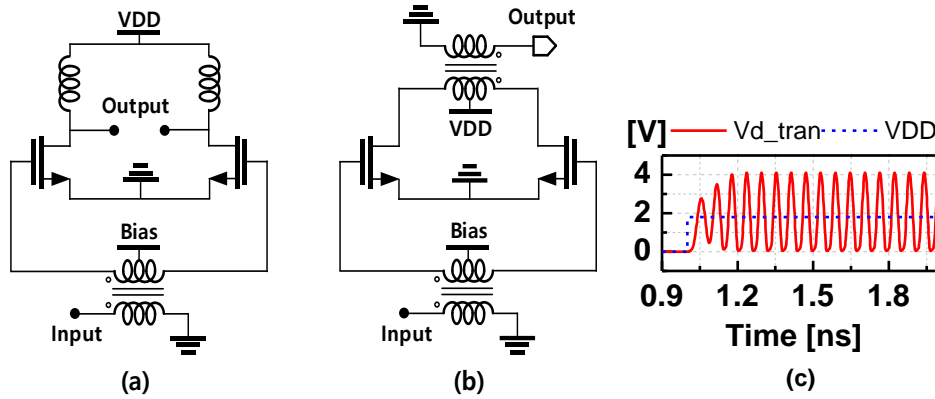


Figure 2.8. Instability in differential amplifiers (a) A pseudo-differential amplifier, (b) a push-pull amplifier, and (c) the simulated oscillation of the drain voltage of a transistor in a push-pull structure after turning on the supply voltage when there is no input signal.

Due to gain compression of the active device in the large-signal domain, the self-oscillation grows exponentially in the transient simulation but is compressed quickly to a particular level. In the large-signal region, where the active devices play as non-linear components of the circuit, stability analysis is necessary to obtain more accurate results. However, the small-signal analysis is more effective when dealing with the unstable mechanism mentioned earlier as it is more intuitive and requires less complexity. To analyze the instability, a simplified schematic of a push-pull PA with a transformer at the input and biasing circuit is illustrated in Figure 2.9(a). Since the instability occurs in a common mode, it can be investigated with the half-circuit, as shown in Figure 2.9(b). Herein,  $L_{cb}$  is the bias line inductance;  $L_{cd}$  is the power supplying line inductance;  $L_{s1}$  and  $L_{p2}$  are the primary coil inductance of the input transformer and secondary coil inductance of the output transformer, respectively.

In Figure 2.9(b),  $L_g = 2L_{cb} + L_{s1}/2$ ,  $r_g = 2R_{cb} + R_{s1}/2$ ,  $L_d = 2L_{cd} + L_{p2}/2$ , and  $r_d = 2R_{cd} + R_{p2}/2$ , while the transistor is modeled using a voltage-controlled current source with a transconductance of  $g_m$  combined with three capacitors:  $C_{gs}$ ,  $C_{ds}$ , and  $C_{gd}$  and output resistor  $r_o$ . The load and the source impedances are not shown in the CM oscillation. A simplified circuit of Figure 2.9(b) is exhibited in Figure 2.9(c) with the two pseudo-voltages  $V_1$  and  $V_2$  for triggering. Herein,  $Z_g$  represents  $r_g + sL_g$ ,  $Z_{gd}$  stands for  $1/sC_{gd}$ , and  $Z_d$  includes  $1/sC_{ds} // r_o // (sL_d + r_d)$ . Subsequently, in the complex-frequency ( $s$ ) domain, the impedances can be expressed as

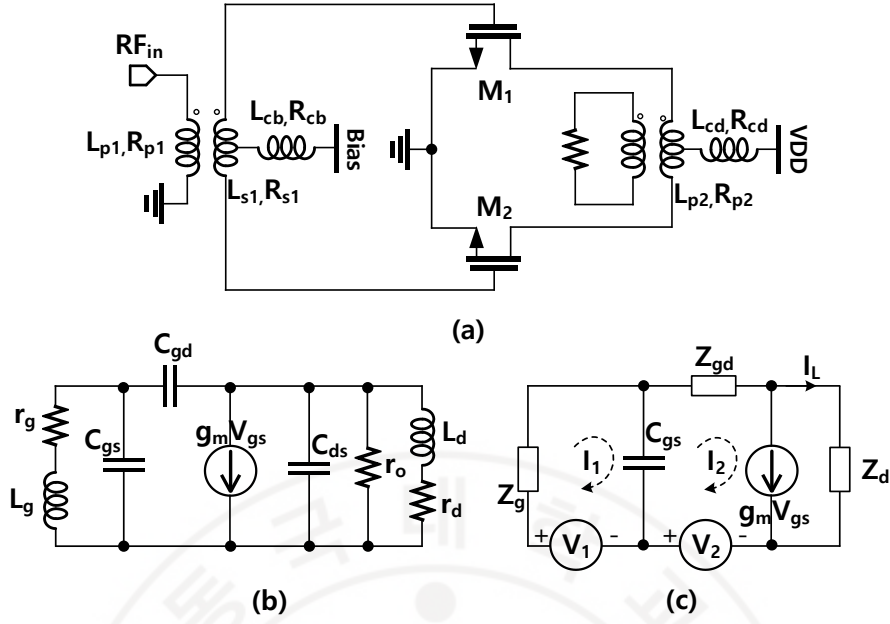


Figure 2.9. Common-mode equivalent circuit of push-pull amplifiers (a) a schematic of the push-pull amplifier, (b) the small-signal common-mode half-circuit of the PA, and (c) a simplified version of the circuit in (b).

$$Z_g = sL_g + r_g; Z_{gd} = \frac{1}{sC_{gd}}; Z_d = \frac{1}{sC_{ds} + \frac{1}{r_o} + \frac{1}{sL_d + r_d}} \quad (2.4)$$

Using Kirchoff's voltage and current laws for the circuit in Figure 2.9(c) with a mark that the current flow through  $Z_L$  is  $I_L = I_2 - g_m V_{gs}$ , we can obtain network equations as

$$[Z][I] = [V]; \text{ where } Z = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}; I = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}; V = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (2.5)$$

$Z$ ,  $I$ , and  $V$  are the impedance, the circulating current, and the voltage matrices, respectively, In Figure 2.9(c), the elements in the impedance matrix can be calculated as

$$\begin{aligned} z_{11} &= Z_g + Z_{gs}; \quad z_{12} = -Z_{gs} \\ z_{21} &= -\left( Z_{gs} + Z_d Z_{gs} g_m \right) \\ z_{22} &= Z_{gd} + Z_{gs} + Z_d + Z_d Z_{gs} g_m, \end{aligned} \quad (2.6)$$



where  $Z_{gs} = 1/(sC_{gs})$ . The circuit can be excited by applying delta functions to  $V_1$  and  $V_2$  to check the current responses in the circuit. In the  $s$  domain, the delta function is expressed as unity; then the circulating currents can be calculated by

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{\det(\mathbf{Z})} \begin{bmatrix} z_{22} & -z_{12} \\ -z_{21} & z_{11} \end{bmatrix} \begin{bmatrix} 1 \\ 1 \end{bmatrix}. \quad (2.7)$$

If the expression of the currents in the  $s$  domain contains right half-plane poles (RHPs), its transformation to the time domain will contain oscillations growing exponentially, resulting in an unstable design. Note that the expressions for the poles are not dependent on the triggering matrix  $[\mathbf{V}]$ . There are two cases when this can happen:  $\det(\mathbf{Z})$  has a right half-plane zero (RHZ), or an element of the  $\mathbf{Z}$  matrix has RHPs. However, the passive components cannot be unstable by themselves, thus we can envisage a situation when a given circuit becomes unstable if  $\det(\mathbf{Z})$  contains RHZs and the imaginary part of the zeros comprises the angular frequencies of the oscillations. The expression of  $\det(\mathbf{Z})$  is given by

$$\det(\mathbf{Z}) = z_{11}z_{22} - z_{21}z_{12} \quad (2.8)$$

By replacing (2.4) with (2.6), and using (2.8), we can obtain the following equation when  $r_o$  is large enough to be ignored, i.e.

$$\det(\mathbf{Z}) = \frac{A(s)}{B(s)} = \frac{a_4s^4 + a_3s^3 + a_2s^2 + a_1s + 1}{s^2C_{gd}C_{gs}(s^2C_{ds}L_d + sC_{ds}r_d + 1)} \quad (2.9)$$

Where

$$\begin{aligned} a_4 &= L_g L_d C_{gds} \\ a_3 &= (r_d L_g + r_g L_d) C_{gds} + g_m C_{gd} L_d L_g \\ a_2 &= L_d L_g C_{gds} + L_g (C_{gs} + C_{gd}) + L_d (C_{ds} + C_{gd}) + g_m C_{gd} (r_d L_g + L_d r_g) \\ a_1 &= r_g (C_{gs} + C_{gd}) + r_d (C_{ds} + C_{gd}) + g_m C_{gd} r_d r_g \\ C_{gds} &= (C_{gs} C_{ds} + C_{gd} C_{ds} + C_{gd} C_{gs}) \end{aligned} \quad (2.10)$$

The solution to  $A(s) = 0$  gives us the zeros of  $\det(\mathbf{Z})$ . It is known that RHZs always come as a pair given as  $s = \alpha \pm j\omega$  in  $A(s)$ , which is a quartic function. Thus, it may potentially have two pairs of solutions that give two oscillation frequencies. Let us consider the circuit in Figure 12(b) by choosing the drain inductance ( $L_d$ ) of 250 pH. If it has an effective quality factor ( $Q_e$ ) of 10 at 10 GHz (the  $Q_e$  at a particular frequency is calculated using  $Q_e = \omega L_d / r_d$ ),



the parasitic drain resistance ( $r_d$ ) is  $1.57 \Omega$ . The gate inductance ( $L_g$ ) and gate parasitic resistance ( $r_g$ ) were chosen to be the same as for the drain inductance:  $L_g = 250 \text{ pH}$  and  $r_g = 1.57 \Omega$ . These inductances are from the routing lines as well as the CM inductance of the input balun used for biasing the transistor. Under given bias conditions, the small-signal parameters of the NMOS device of  $90 \times 0.18 \mu\text{m}$  were extracted as  $C_{ds} = 52.9 \text{ fF}$ ,  $C_{gs} = 99.7 \text{ fF}$ ,  $C_{gd} = 29.4 \text{ fF}$ ,  $g_m = 38.7 \text{ mS}$ , and  $r_o = 549 \Omega$ . Using the equation for  $A(s)$  in (6), we can see four zeros in  $A(s)$ :  $s_{12} = 40.93 \times 2\pi(-0.34 \pm j) \text{ Grad/s}$  and  $s_{34} = 23.46 \times 2\pi(0.15 \pm j) \text{ Grad/s}$ , which means that the circuit oscillates at  $F = 23.46 \text{ GHz}$ . If  $r_o$  is taken into account, the calculated  $F$  is shifted to  $23.49 \text{ GHz}$ . In the simulation, we obtained  $F = 25.81 \text{ GHz}$ , which was slightly higher than the calculated value. It should be noted that the calculated CM oscillation frequency was quite similar to the simulated value with the simplified small-signal model of the MOS transistor even though the MOS behaves as a non-linear component when the oscillation starts since it is operating in the large-signal domain.

It can be concluded that  $L_d$ ,  $L_g$ , and  $C_{gd}$  are the components mainly taking charge informing the positive feedback for the active device. Both in the simulation and calculation, the oscillation turns off if either  $L_d$  or  $L_g$  becomes zero or infinite. When  $L_g = 0$  and  $r_g = 0$ , the active device becomes inactive, and no oscillation can remain since the gate voltage becomes zero. When there is no gate inductance (i.e.,  $L_g$  is infinite), the drain voltage ( $V_d$ ) and the gate voltage ( $V_g$ ) are in phase due to a capacitive divider formed by  $C_{gd}$  and  $C_{gs}$ , as shown in Figure 12(b). Therefore, no oscillation can remain in this case as well. In a real case, the CM inductances  $L_d$  and  $L_g$  always exist, thereby degrading amplifier stability. Therefore, we investigated several ways of preventing CM oscillation.

### 2.3.3 Stabilization methods for differential amplifiers

#### a) The Effect of CM Inductance on Stability

Figure 2.10 presents a comparison between the simulated and calculated oscillation frequencies as a function of  $r_g$  for two cases:  $L_g = L_d = 250 \text{ pH}$  and  $r_d = 1.57 \Omega$ , and  $L_g = L_d = 500 \text{ pH}$  and  $r_d = 3.14 \Omega$ . As expected, the oscillation frequency depended weakly on  $r_g$ , and the oscillation stopped when  $r_g$  was larger than a specific value,  $R_{g\text{off}}$ . In the same way, increasing  $r_d$  also improved the stability of the amplifier. However,  $r_d$  should be kept as small as possible for better efficiency since the drain current is conducted throughout it. In this case, a decoupling capacitor can be included in the center tap of the winding inductor at

the drain to resonate out the CM coil inductance  $L_d$ . To achieve better stability, de-Qing the bypass capacitor is also recommended by employing an additional resistor in series with it.

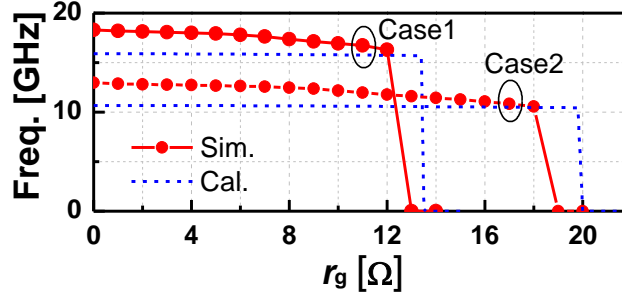


Figure 2.10. Calculated and simulated oscillation frequencies versus  $R_g$ : Case 1:  $L_g=L_d=250$  pH and Case 2:  $L_g=L_d=500$  pH.

The bias resistor can usually be chosen to be much larger than the range of  $R_{g\text{off}}$  so that the oscillation can be effectively prohibited. In this case, the effect of the bias path on the CM oscillation is only minor and can be ignored. However, the base bias resistor should be kept small enough to conduct the DC base current for bipolar-junction-transistor (BJT) amplifiers. The minimum required gate (base) resistance ( $R_{g(b)\text{off}}$ ) was calculated and compared to the simulation results, as shown in Figure 2.11.

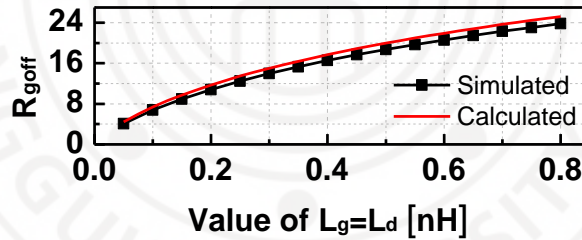


Figure 2.11. Calculated and simulated gate resistances which prohibited the unstable oscillations ( $R_d=(2\pi\times 10G\times L_d)/10$ ).

*b) The effect of the coupling capacitance between the coils*

Typically, two coils are placed in proximity to achieve strong magnetic coupling to obtain a high-efficiency on-chip transformer. The narrow gap between the two coils results in significant parasitic capacitance between the two windings even though it is distributed over the entire length of the two winding coils. We can use a lumped capacitor connected between two central points of the two coils to investigate its effect on the stability of the circuit, as depicted in Figure 2.12.

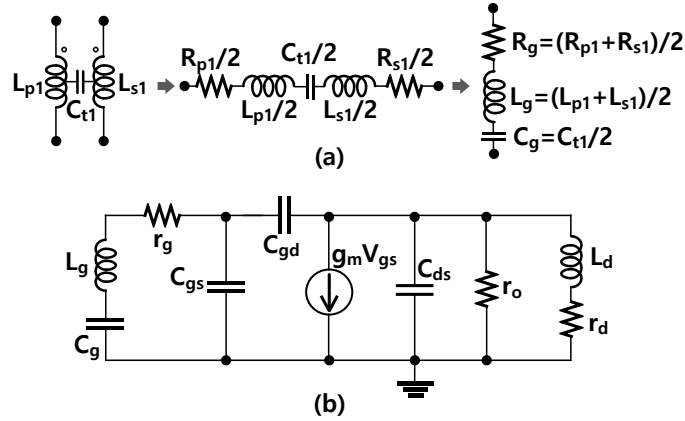


Figure 2.12. Effect of the coupling capacitance between the coils of the TF (a) the parasitic capacitance between the two coils of the input transformer and (b) the small-signal CM half-circuit of the PA.

It is interesting to observe that the push-pull amplifier may experience instability because of the capacitance between the two coils of the input transformer. The series coupling capacitor between the two coils of the input transformer ( $C_{t1}$ ) can form a closed path for the CM oscillation. Let us add a gate capacitor ( $C_g = C_{t1}/2$ ) to the half-circuit of the CM operation, as shown in Figure 2.12(b). When we ignore the bias path, the gate resistor and inductor can now be calculated as  $r_g = (R_{s1} + R_{p1})/2$  and  $L_g = (L_{s1} + L_{p1})/2$  (Fig. 2.12(a)). The analysis in the previous section can be applied when substituting  $Z_g$  given in (2.4) by

$$Z_g = sL_g + r_g + \frac{1}{sC_g} \quad (2.11)$$

Using the new  $Z_g$  to calculate the elements of the impedance matrix  $\mathbf{Z}$  given in (2.17) and then replacing these values in (2.8), we can obtain a new expression for the numerator of  $\det(\mathbf{Z})$ , represented by  $A(s)$ . As an example, if  $L_g = 300$  pH,  $L_d = 200$  pH,  $r_g$  and  $r_d$  are chosen so that the  $Q_e$  of their inductance is 15 at 20 GHz,  $C_{t1} = 150$  fF, and the MOS transistor size is  $90 \times 0.18\mu\text{m}$  with  $C_{ds} = 52.9$  fF,  $C_{gs} = 99.7$  fF,  $C_{gd} = 29.4$  fF,  $g_m = 38.7$  mS, and  $r_o = 549$   $\Omega$ , the solutions of the equation  $A(s) = 0$  are  $s_{12} = 2\pi \times 44.3 \times (-0.32 \pm j)$  Grad/s and  $s_{34} = 2\pi \times 30.72\text{G} \times (0.06 \pm j)$  Grad/s. Thus, there is a CM oscillation at the frequency of 30.72 GHz. The simulation results showed an oscillation at 31.62 GHz, which is slightly higher than the calculated value. Figure 2.13 contains a plot of the variation in oscillation frequency versus  $C_{t1}$  for two cases:  $L_g = 300$  pH,  $r_g = 2.51$   $\Omega$ ,  $L_d = 200$  pH, and  $r_d = 1.67$   $\Omega$  and  $L_g = 600$  pH,  $r_g = 5.02$   $\Omega$ ,  $L_d = 400$  pH, and  $r_d = 3.34$   $\Omega$ . The calculated values were in good agreement with the simulation, both showed that the CM oscillation stopped when  $C_{t1}$

was smaller than a certain value. For example, in case 2, when the calculated  $C_{t1} = 70$  fF, the oscillation was not triggered while the minimum series capacitance was around 75–100 fF in the simulation.

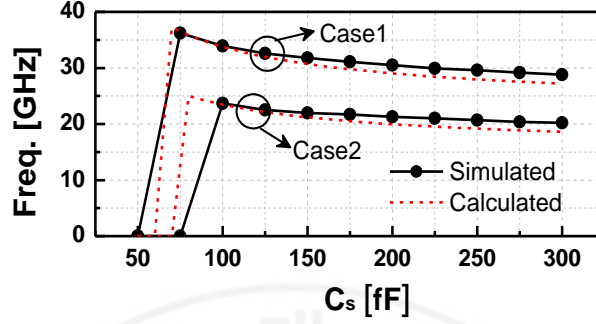


Figure 2.13. The calculated and simulated oscillation frequencies versus  $C_g$ : **Case 1:**  $L_g=300$  pH,  $L_d=200$  pH and **Case 2:**  $L_g=600$  pH,  $L_d=400$  pH.

To further prevent instability, we can increase the resistive loss by increasing  $r_d$  and  $r_g$  or decrease the capacitive coupling by reducing  $C_g$ . However, these component values should not be set as a trade-off in a practical design. Thus, any additional resistors must be avoided in the signal path to guarantee the high power efficiency of the designed PA. It should be noticed that even though the resistive losses in the system could be chosen barely enough to suppress the oscillation, a small damping factor in the analytical solution forecasts a considerably long settling time of the PA, which should also be avoided with the proposed analysis method.

### c) Series RC feedback network

Using a resistive feedback network by connecting a resistor ( $R_{fb}$ ) between the gate and the drain of the transistor can compress the gain of the system, which helps to mitigate instability. The feedback resistor is typically connected in series with a capacitor ( $C_{fb}$ ) to provide bias voltages for the gate and the drain independently, as illustrated in Figure 2.14. The calculation for this case with the proposed method is directly applicable if  $Z_{gd}$  in (2.4) is replaced by

$$Z_{gd} = \frac{\frac{1}{sC_{gd}} \left( \frac{1}{sC_{fb}} + R_{fb} \right)}{\frac{1}{sC_{gd}} + \frac{1}{sC_{fb}} + R_{fb}} \quad (2.12)$$

The expression of  $Z_g$  is still the same as in (2.11). The numerator of  $\det(\mathbf{Z})$ , i.e.  $A(s)$ , is now a quintic polynomial with an additional real zero. For example, if  $L_g = 300$  pH,  $r_g = 2.51$   $\Omega$ ,  $L_d = 200$  pH,  $r_d = 1.67$   $\Omega$ ,  $C_g = 100$  fF,  $C_{fb} = 200$  fF,  $R_{fb} = 800$   $\Omega$ , and the MOS transistor size is  $90 \times 0.18$   $\mu\text{m}$  with the parameters given in the previous section, the solutions of the equation  $A(s) = 0$  are  $s_{12} = 2\pi \times 46.28 \times (-0.27 \pm j)$  Grad/s,  $s_{34} = 2\pi \times 33.71 \times (0.03 \pm j)$  Grad/s, and  $s_5 = -1.16 \times 10^{10}$  rad/s. This means that there is a CM oscillation at 33.71 GHz, which is quite close to the simulation value of 33.67 GHz.

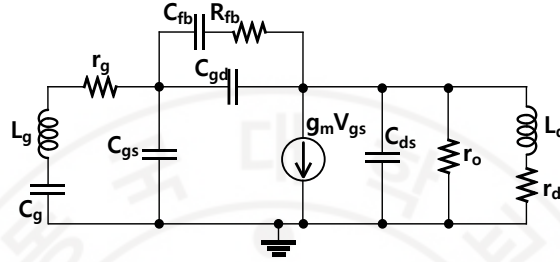


Figure 2.14. A schematic of the common-mode half-circuit push-pull amplifier with an RC feedback circuit (the bias circuit is hidden).

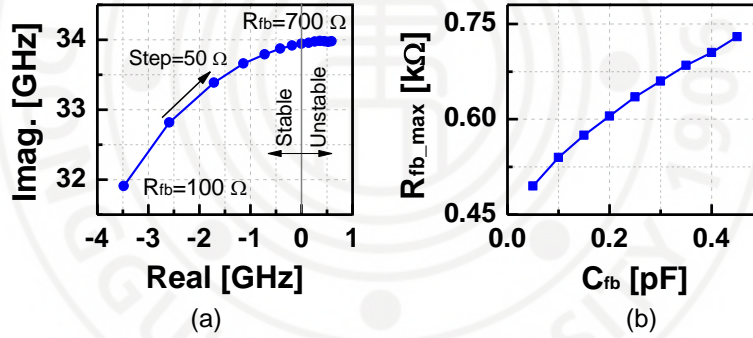


Figure 2.15. (a) The root locus of the point causes instability versus the value of  $R_{fb}$ . (b) The simulated maximum value of  $R_{fb}$  is required to turn off oscillation.

By using the small-signal analysis, the root locus of the system-pole (or the zero of  $\det(\mathbf{Z})$ ) that causes instability in the circuit is plotted as a function of  $R_{fb}$  as shown in Figure 2.15(a). To suppress the oscillation, the value of  $R_{fb}$  should be smaller than a specific value,  $R_{fb(max)}$ , to provide a large enough loss between two  $LC$  tanks at input and output ports as depicted in Figure 2.14. Meanwhile,  $R_{fb}$  must be chosen to be large enough for a better closed-loop gain. In addition,  $R_{fb}$  should not be too small to provide valid resistive feedback for a meaningful power gain. Otherwise, an oscillation happens at a lower frequency as  $C_{fb}$  is effectively added to  $C_{gd}$ . Also, it would significantly reduce the power efficiency as well



as the gain of the PA if the RC feedback is configured with a small  $R_{fb}$  and a large  $C_{fb}$ . Therefore, proper selection of  $R_{fb}$  is essential for a robust PA design with well-balanced RF performance. Figure 2.15(b) shows the maximum value of  $R_{fb}$  ( $R_{fb(max)}$ ) required to stabilize the circuit depending on the value of  $C_{fb}$ . Different from  $r_g$  and  $r_d$ , the critical point maintaining oscillation depends weakly on  $R_{fb}$  since  $R_{fb}$  is not in the main path that creates the CM oscillation. This results in a relatively large error in calculating  $R_{fb(max)}$  using small-signal analysis compared to the value seen from large-signal simulation for suppressing the instability. Therefore, it is recommended to be conservative in selecting  $R_{fb(max)}$  in a practical design.

### 2.3.4 Experimental Verification

It is difficult to validate the established design guidelines using a fully integrated PA in CMOS technology. Instead, the onboard push-pull amplifier presented in Figure 2.8b was implemented using a high-frequency BJT (2N3904) with a cut-off frequency of 300 MHz. The implemented PA is shown in Figure 2.16. The onboard input and output transformers were implemented with a center-tap option so that they could be soldered to any extra inductor to change the CM inductances ( $L_g$  and  $L_d$ ) of the amplifier for verification purposes. At first, each center tap was shorted to GND, as can be seen on the front of the push-pull amplifier in Figure 2.16a. It should be noted that noise from the bias line would affect the amplifier if the bypass capacitors were absent. Moreover, the balance structure would be broken at the operating frequency regime. The applied bypass capacitor was 100  $\mu\text{F}$ , which was large enough to be considered a short circuit in the MHz range (e.g., at 1 MHz, a 100  $\mu\text{F}$  capacitor has a capacitance of  $1.6\text{E-}3 \Omega$ ). The drain voltage waveform of each transistor was directly probed and measured with a digital oscilloscope (Keysight DSOX6002A).

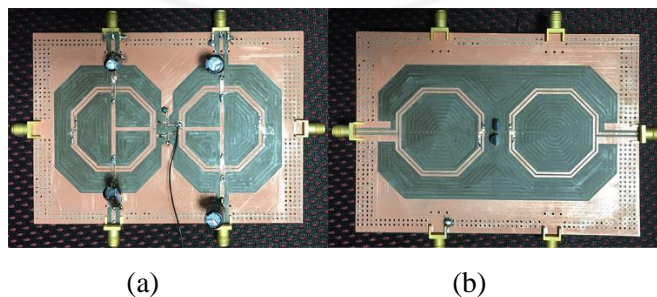


Figure 2.16. The on-board push-pull amplifier. (a) the front side and (b) the backside.



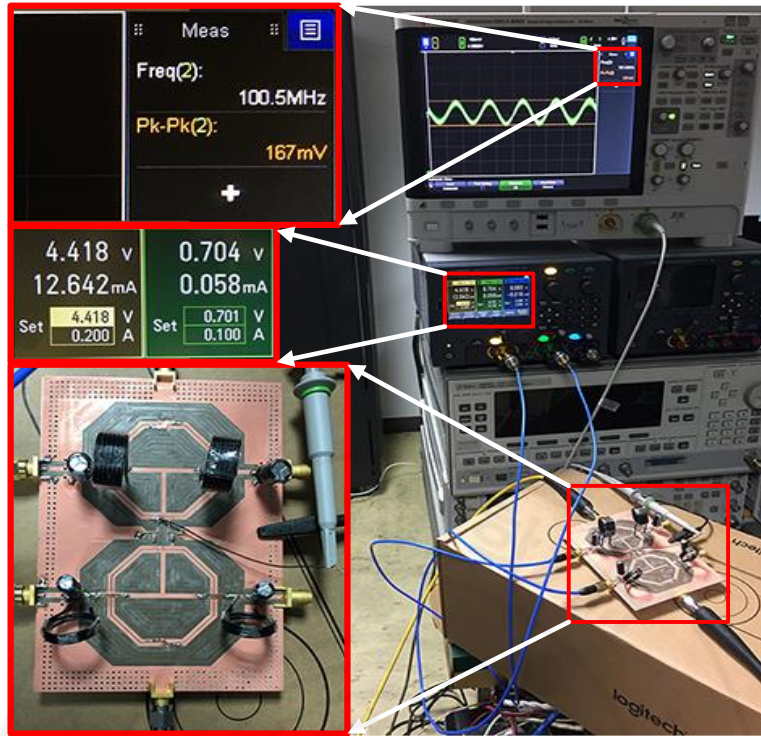


Figure 2.17. Measurement of common-mode oscillation in the push-pull amplifier.

With the original design of the onboard transformers, the CM inductances were so small that the active devices did not sustain any oscillations. However, when  $L_g$  and  $L_d$  were increased with the extra inductors connected to the center tap, it led to instability in the PA under various ranges of bias points. Figure 2.17 presents the measurement setup where the transistors were biased with base current  $I_b = 0.058$  mA and collector current  $I_c = 12.6$  mA under stable conditions. At this bias point, the amplifier had a 7-dB small-signal gain. When we measured the oscillation, the input and output were terminated with  $50 \Omega$ . In the oscilloscope, a sinusoidal voltage swing was observed at the transistor's drain with a frequency of around 100 MHz and a peak-to-peak swing of 167 mV. The output spectrum of the unstable amplifier is given in Figure 2.18a with  $P_{in} = -28$  dBm at 33 MHz. It can be seen that the signal was disturbed by unwanted spurious tones at around 100 MHz along with their second harmonics from the CM oscillation. Following the proposed design guidelines, the amplifier was stabilized as expected by using a base resistor of  $50 \Omega$  (the measured output spectrum is presented in Figure 2.18b).

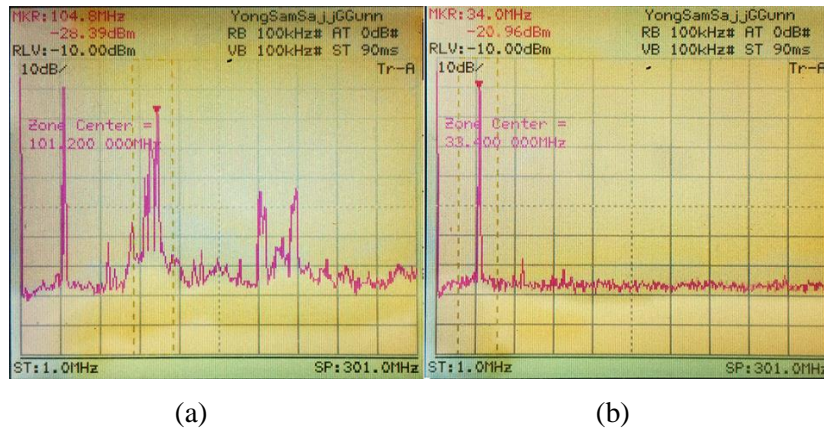


Figure 2.18. Output spectrum before stabilization (a) and after stabilization by using a  $50 \Omega$  resistor at the base bias line (b).

## 2.4 Reference

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### III. X-band transformer-coupled power amplifiers

#### 3.1 Introduction

X-band (8-12GHz) radars and remote communication systems are widely used in military and civilian systems alike. Radars operating within the X-band range of 2.5-4 cm are sensitive to small air particles and can thus be used for short-range climate detection and observation [3.1]-[3.3]. The X-band is also used for industrial communication in both terrestrial and space [3.4]-[3.6]. In particular, Active Electronically Scanned Array (AESA) has been gaining much attention lately due to the potential application of smart radar systems to aircraft vehicles [3.7], and low-cost, electronically steerable short-range weather radars for civilian use [3.8]. Hence, recent research in transmit/receive modules (TRM) in the X-band has shown promise [3.9]-[3.12].

Low-cost AESA systems have a high reliance on PAs because the performance of a PA determines the power consumption, spectral efficiency, and effective range coverage. While GaAs, GaN, and GaN-based PAs provide the higher output power and efficiency of AESA systems, it still requires a back-end module to control the phase and magnitude of Tx/Rx signals. This back-end module is realized as a silicon-based device with the ability to drive the output power beyond 20 dBm [3.13]. As mentioned in [3.14], [3.15], it is always desirable to integrate a PA in a single CMOS chip for a lower cost and reduced size in a low-cost, short-range radar or communication system. Therefore, high-performance CMOS PAs in the X-band are gaining intense interest [3.16]-[3.25]. PA design in a nanoscale CMOS process is technically challenging because of serious second-order effects and reduced breakdown voltages.

For silicon-on-insulator (SOI) CMOS PA design, stacking multiple FET devices to allow higher supply voltage is a topology that enhances the output power. A similar approach can be applied to stacked transistors in a triple-well process with just two transistors [3.22]. Using power combining techniques is also a popular method for increasing the PA's output. By merely increasing the transistor size, the high output power cannot be achieved due to the unrealistically small optimum output resistance ( $R_{opt}$ ) of the active device [3.26]-[3.27]. Using the current combining technique (CCT), one can increase the inductance of the passive components to resonate capacitive parasitics at the nodes of the transistors.



When large devices are used, it does not achieve a transformation gain benefit from the overall resistance of the device [3.28], resulting in a poor output impedance matching [3.17], [3.24], which degrades power efficiency. Comparatively, an  $m$ -way voltage power combining scheme produces a ratio of  $m^2$ -times for the load seen through the transistors' output. This means that the voltage combining technique (VCT) supports the larger device size without compromising output matching [3.28]. CMOS PAs often use a compact, high-efficiency push-pull structure, which can be viewed as a PA with a two-way voltage power combiner. Although the VCT has several advantages, high-way voltage power combiners (PCs) are still quite rare in X-band PAs, except for those with four-way voltage PCs [3.20], [3.24].

In section 3.2, we present a PA in X-band with an attained figure-of-merit of 85.0 dBm.Hz<sup>2</sup>. This is the highest FoM we have ever seen in CMOS PAs, and it is comparable to SiGe PAs around X-band. This amplifier consists of three two-stage push-pull amplifiers whose output powers are combined in the voltage domain by a voltage power combiner (PC).

For a push-pull power amplifier, a large transformation ratio of the TF (i.e.  $n>1$ ) can be used to support a large device size and further boosts the output power of the PA. In our work as presented in section 3.3, we employed a 1:2 TF at the output stage to obtain a PA design based on the cascade of two triple-well transistors to achieve high power efficiency [3.22].

In section 3.4, a two-stage class-AB PA is presented with a transformer-based matching network as the input stage and a compact transformer at the output as the power combiner. Such a structure provides efficient output power combining while avoiding possible instability. Power combining comprises adding the output voltages of several power amplifiers, and it is simple enough to be applied at high frequencies.

### **3.2 Power amplifier design using voltage and current power combining**

The entire schematic of the proposed two-stage PA using six-way voltage power combination in the X-band is illustrated in Figure 3.1. The PA has power stage and driving stage. The power stage includes three same push-pull PA cells whose outputs are combined in the voltage domain using a three-way power combiner. The three driving amplifiers (DAs) use push-pull amplifying configuration with an input power splitter.

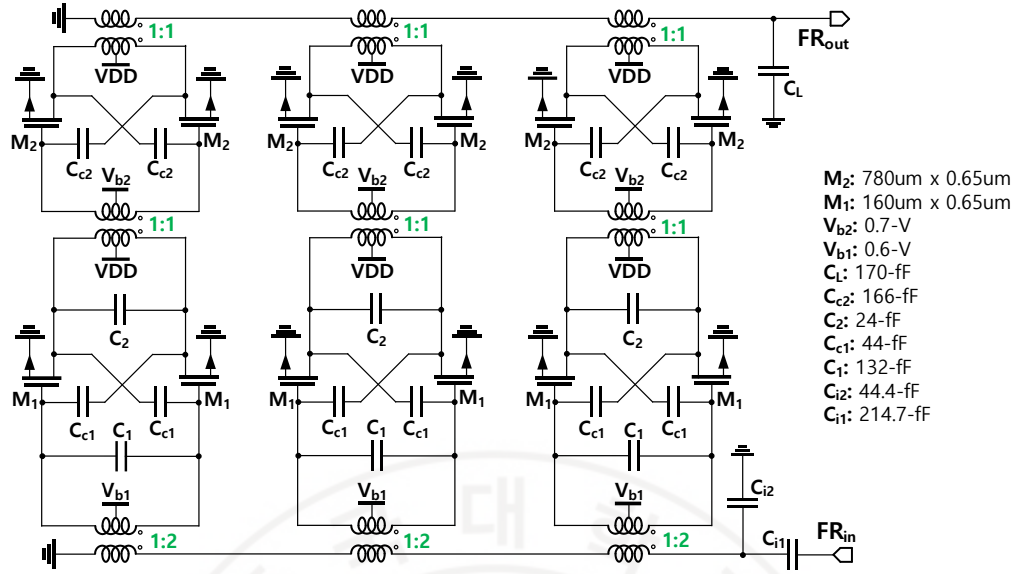


Figure 3.1. Full schematic of the X-band two-stage PA using six-way power combination.

### 3.2.1 Architecture consideration

To design a high output power PA, the use of power combining techniques including current combining technique (CCT) and voltage combining technique (VCT) were considered as presented in Figure 3.2. An  $m$ -way differential-to-single-ended current mode power combiner based on ideal  $1:n$  TFs supports an optimum resistance for each device of  $R_{opt}=m \times R_L / 2n^2$ , where  $R_L$  is the load resistance with the typical value of  $50 \Omega$  [3.28]. When  $n=1$ , this value becomes  $R_{opt}=m \times R_L / 2$ . The denominator of 2 can be viewed as the effect of the two-way voltage combining push-pull structure. The effective  $R_{opt}$  of the total  $2 \times m$  number of devices connected in parallel is calculated to be  $R_{opt\_total}=R_L / 4$ . This means that the use of CCT does not affect the optimal total device size. By contrast, an ideal  $m$ -way  $1:1$ -TF-based voltage mode power combiner requires a total optimum device resistance of  $R_{opt\_total}=R_L / (2 \times m)^2$ , supporting a larger output device size while remaining a good power matching at the load. As a reasonable voltage combining, a three-way power combining/splitting structure ( $m=3$ ) was chosen in this design to support an appropriately large device aiming at a high-efficiency layout realization of the output transistor.

The power combiner (PC) and splitter (PS) were implemented using the ultra-thick metal (UTM) layer for the primary coils and the combination of the two metal layers below the UTM for the secondary coils. A 3-D view of the combiner and splitter simulated on HFSS is shown in Figure 3.3. As for the PC, the UTM is used for the primary coils to conduct



the large quiescent drain currents of the output transistors. The supply voltage (VDD) was provided from several positions to reduce the parasitic series resistance between VDD and the drain of NMOS which can cause a serious voltage drop when the total bias current is large.

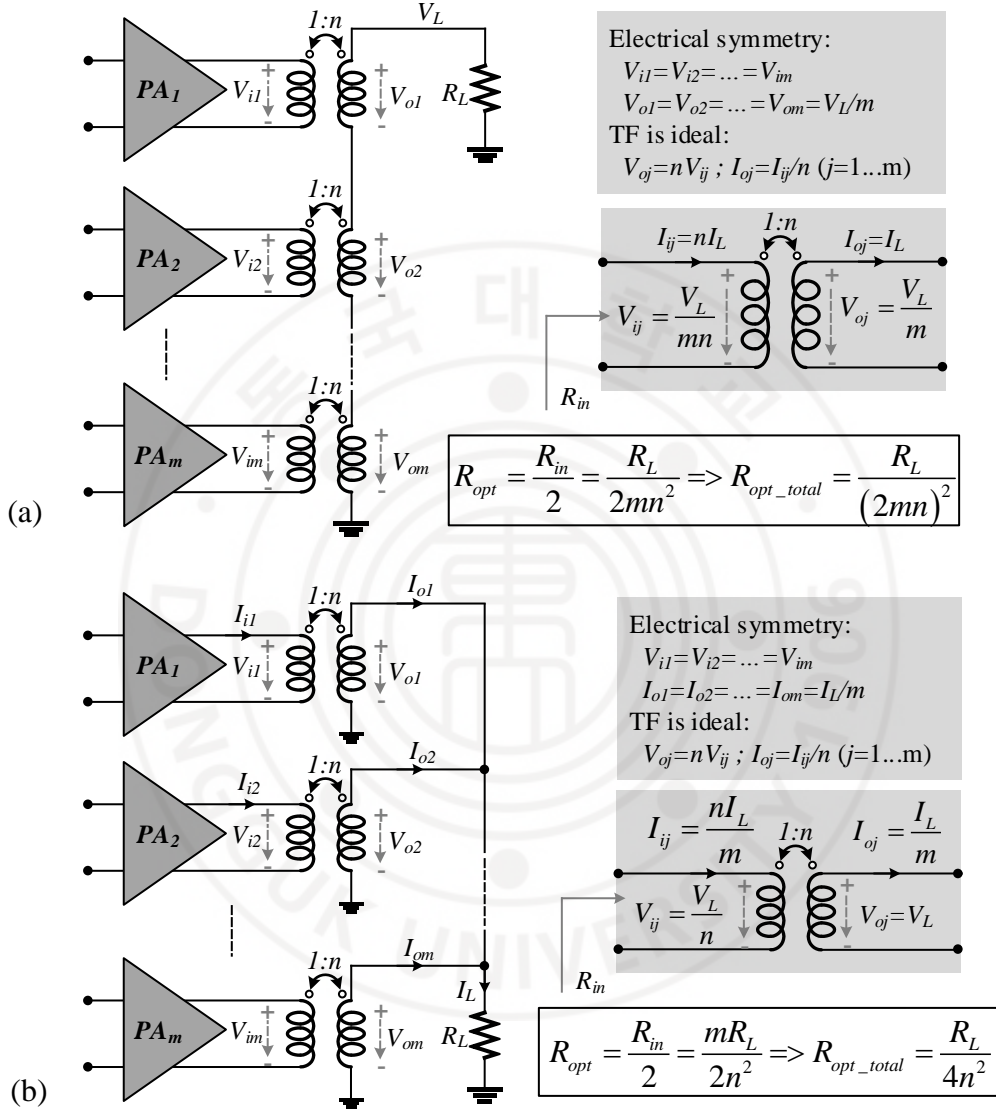


Figure 3.2. Conventional TF-based voltage combiners (a) and current combiners (b).

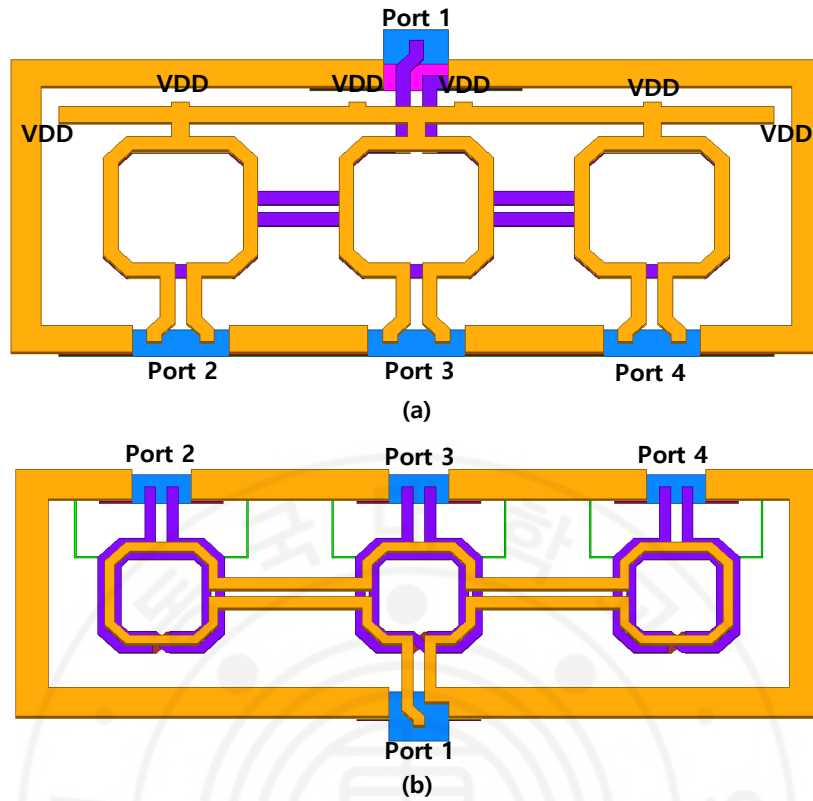


Figure 3.3 HFSS implementations of the power combiner (a) and power splitter (b).

When we use the voltage combining/splitting technique, one of the concerns is to keep the electrical symmetry between the combined paths. If the combiner or splitter operates close to its SRF, it may cause an imbalance in amplitude and phase between signal paths which seriously degrades the combining efficiency. Thus, it is necessary to perform the EM simulation with HFSS to verify if there is no asymmetry issue in the designed structure. Figure 3.4a shows the simulation results of the phase and amplitude imbalance of the power combining network. As illustrated in Figure 3.4a, the imbalance between signal paths becomes serious when the frequency is larger than 20-GHz. The phase imbalance is smaller than  $6^\circ$  and the amplitude imbalance is within 0.5-dB from 0.5-GHz to 20-GHz. Also, the simulation imbalances of the phase and the amplitude between signal paths for the input PS is shown in Figure 3.4b, and the simulated results are also quite small in the X-band. The simulated results confirmed that the proposed three-way power combining/splitting architecture demonstrates electrically symmetric RF signal paths in the band of interest.

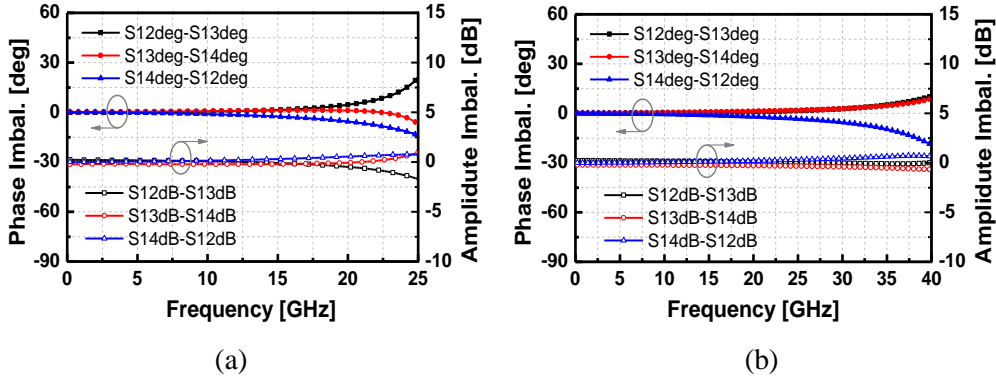


Figure 3.4. Simulated phase/amplitude imbalances of the (a) output 3-way power combiner and (b) input 3-way power splitter.

### 3.2.2 Stabilizing push-pull amplifiers

The proposed PA was built based on the push-pull amplifier structure which provides several important benefits of high efficiency and high output power while occupying a compact area. However, the differential two-port composed of two common source amplifiers is conditionally unstable in the low-frequency region due to the unwanted feedback caused by the gate-to-drain parasitic capacitor  $C_{gd}$ . One method to stabilize the differential pair of transistors is to use a resistor connected in series with a capacitor in the feedback path from the drains to the gates (RC-feedback) to intentionally increase the resistive loss for the stabilization [3.18], [3.22]. However, the drawback of this technique lies in its side effect on the degradation of power efficiency, preventing it from being widely used, especially at high frequencies. A feedback network using inductors was used to resonate out  $C_{gd}$  for a stabilized push-pull amplifier while attaining an improved efficiency owing to the high-quality factor of inductors realized at high frequency [3.29]. However, the large area occupancy of the inductive feedback is not appealing for architecture using a power combining technique, specifically in the low-frequency regime. A more common technique for the stabilizing task is to use a pair of capacitors cross-connected between the drains and the gates of the two active devices to neutralize the gate-to-drain parasitic  $C_{gd}$ . In this proposed PA design, we employed cross-connected couples of neutralizing capacitors ( $C_{neu}$ ) to stabilize the push-pull amplifiers both in the power and the driving stages to attain improved efficiency. The value of the neutralizing capacitor is ideally estimated to be the same as the  $C_{gd}$  of the transistor [3.30]. In designing the unit cell of the PA,  $C_{neu}$  was tuned around  $C_{gd}$  and the maximum available gain ( $G_{ma}$ ) and the stability factor (K-factor) were investigated to determine the final value of  $C_{neu}$ .

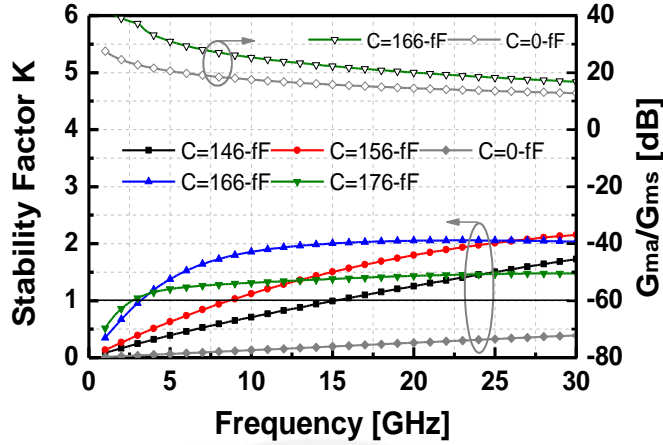


Figure 3.5. Simulated  $G_{ms}/G_{ma}$  and stability factor  $K$  versus frequency of several values of the neutralization capacitor ( $C_{neu}$ ).

Figure 3.5 shows the maximum available gain ( $G_{ma}$ ), maximum stable gain ( $G_{ms}$ ), and the stability factor ( $K$ ) of the differential pair in the power stage with various values of  $C_{neu}$ . Herein,  $\Delta$  was also examined to ensure its absolute value is less than unity. Without using a neutralization capacitor, the active differential pair is conditionally unstable with  $K < 1$  in the band of interest. It is noteworthy that the amplifier without  $C_{neu}$  becomes stable after a specific frequency of 7.7-GHz from the simulated K-factor versus frequency, which is also called knee frequency. When  $C_{neu}$  is involved, the knee frequency decreases as  $C_{neu}$  increases. However, when  $C_{neu}$  becomes even larger, it works as an AC-coupling capacitor, then the differential pair becomes the cross-coupled pair which is widely used in oscillator designs. In this case, the knee frequency of the differential pair increases as  $C_{neu}$  further increases. As shown in Figure 5, when  $C_{neu}$  of 146-fF, 156-fF, and 166-fF is used, the knee frequency is reduced to around 15-GHz, 7-GHz, and 3-GHz, respectively. When  $C_{neu}$  equals 176-fF, the knee frequency is around 2.7-GHz. If  $C_{neu}$  further increases, the knee frequency was seen to be increased as we noticed. In this design,  $C_{neu}=166$ -fF was determined to achieve a stable condition in the X-band. This also makes the design less sensitive to the parasitic variations of the device. Similarly,  $C_{neu}=44$ -fF was chosen for the differential pair in the driving stage.

### 3.2.3 Gate bias voltage consideration

When we design the output stage of the PA with the output PC, choosing an appropriate size of the active device and the matching network is crucial to achieving the desired output power with an enhanced power efficiency owing to its dominance in power consumption compared to the driving stage. The first mission is to choose the gate bias voltage for the

output transistor since it is relatively independent of the active device size. The feasible range of output device size is determined by the load resistance and the power combining scheme. Hence, it is unrealistic to increase the output power by merely increasing the output device size considering the matching difficulty and bandwidth. Therefore, the gate bias for the output transistors should be chosen to achieve a good tradeoff between the maximum achievable output power and power efficiency.

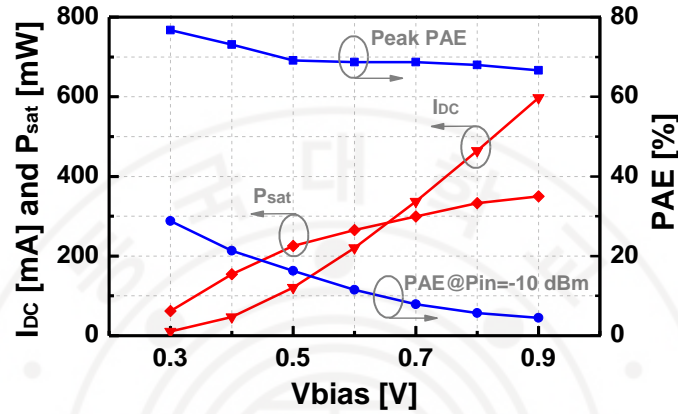


Figure 3.6. Simulated peak PAE, PAE at  $P_{in}=-10$ -dBm, saturated output power ( $P_{sat}$ ), and DC current consumption ( $I_{DC}$ ) of the output transistor differential amplifier versus the gate bias voltage ( $V_{bias}$ ).

We performed the harmonic balance (HB) simulation using Spectre to investigate the large-signal performances of the output transistor cell depending on the gate bias voltage. Figure 3.6 shows the maximum output power ( $P_{sat}$ ), the peak power added efficiency (PAE), the PAE at  $P_{in}=-10$  dBm, and the quiescent current consumption of the differential two-port at the output stage versus the gate bias voltage ( $V_{bias}$ ). In this simulation, the post-layout RC extraction was performed with Calibre. As can be seen,  $P_{sat}$  increases monotonously versus  $V_{bias}$ , and its increment becomes compressed in the large bias region. The peak PAE generally reduces when  $V_{bias}$  increases.

However, the decrease is quite minor when  $V_{bias}$  is larger than 0.5-V, and the peak PAE keeps almost close to 70%. This means that when the input signal is large enough, the shape of the voltage waveform on the gate does not depend much on its DC bias voltage. The active devices operate as switches in the large-signal regime, which is inherently the working principle in switching PAs such as class  $D^{+1/-1}$ ,  $E^{+1/-1}$ ,  $F^{+1/-1}$ , particularly when the applied gate bias is small. However, the relative independence of the PAE from the gate bias voltage does not remain when the input power ( $P_{in}$ ) is small. For example, at  $P_{in}=-10$  dBm,

the plot of the PAE drops drastically as  $V_{bias}$  increases. The large DC current consumption at the large gate bias makes the differential amplifier less efficient in the small-signal regime. Based on this experiment, the gate bias voltage of 0.7-V was chosen for the output transistor to achieve a good output power with a moderate level of DC current consumption and power efficiency at the small signals. Designing the gate bias voltage for the driving stage was also performed similarly to the power stage. The trend of the performance versus  $V_{bias}$  in the driving stage was similar to the power stage except that the output power criterion of the driving stage was mitigated compared with the power stage. Thus,  $V_{bias}$  equal to 0.6-V was chosen for the driving stage to further enhance the power efficiency with an improved gain.

### 3.2.4 Device sizing and impedance matching

In the output stage, the TF-based power combiner has to transfer the 50- $\Omega$  output load to the optimum impedance of each differential pair to maximize the output power generated by the active device. The impedance seen from the load toward the active device should be also close to 50- $\Omega$  to minimize the return loss at the output port. From the calculation of the optimum resistance for the output, transistor mentioned previously, the calculated  $R_{opt}$  of each transistor cell is  $50/(2 \times 3) = 8.3\text{-}\Omega$ , or the  $R_{opt}$  of each differential pair amplifier is 16.6- $\Omega$ . This calculation is under the assumption that the TFs are ideal with the coupling factor of 1, and the inductances of the TF are resonated out by corresponding ideal capacitors.

In the real case, the winding coils composing the TF have their own resistive losses, and the mutual coupling factor is smaller than 1. Figure 3.7a shows the impedance matching schematic of the output stage including the PC composed of three TFs, the 50- $\Omega$  load connected in parallel with a matching capacitor  $C_L$  and the output impedance of the differential amplifiers is modeled by a resistor in parallel with a capacitor. Since the electrical symmetry of the PC is already verified, we can assume that the three TFs composing the PC are all identical, and the voltages at the three input ports are the same. From the circuit theory, it is known that the nodes whose voltages are the same can be connected without changing the characteristics of the whole circuit. Applying the theory in this case, the three input ports of the PC can be connected to form a single input port with the correspondingly scaled R and C in parallel as shown in Figure 3.7b. Now the three-way PC can be characterized by an equivalent two-port TF whose primary inductance is reduced by three times and secondary inductance is tripled compared to those of the single unit TF



composing the original PC. With this equivalent TF model, we can choose its optimum source and load impedances given by the equation (2.1).

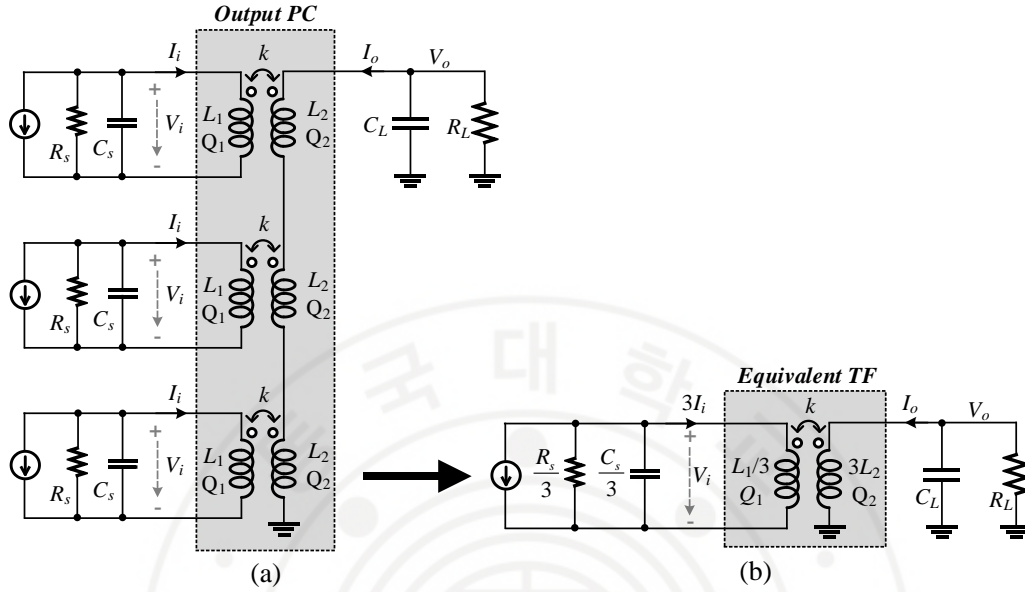


Figure 3.7. Schematic (a) and the equivalent TF model (b) of the output stage.

Table 3.1. Characteristic parameters of the equivalent TF of the output PC at 10-GHz.

$L_1$	$L_2$	$Q_1$	$Q_2$	$k$
80.5 pH	815 pH	8.1	5.9	0.76

It should be noticed that the calculated source impedance at the input side of the equivalent TF has to be tripled to get the optimal source impedance of each input port of the original three-way PC. Hence, the source impedance of each input port of the PC is  $3 \times Z_{sopt}$ . The characteristic parameters of the equivalent TF of the output PC extracted at 10 GHz are given in Table 3.1. As can be seen, the ratio between  $L_2$  and  $L_1$  is around 10, implying an equivalent turn-ratio of approximately three as expected. By using (2.1), the output PC was co-designed with an output active device with a gate width of 780- $\mu\text{m}$  so that the calculated optimum impedances at the input and output sides were close to their corresponding practical source and load. The synthesized optimum output resistance is around 50- $\Omega$  which allows us to simplify the output matching network which is only with a resonating capacitor connected in parallel to the load. A good impedance matching level was achieved at the

load side with the simulated  $S_{22}$  of nearly -30 dB. Performing physical layout for such a big output transistor was also an important task, affecting the performance of the transistor cell. In this work, the fishbone layout structure was applied for the output transistor to reduce the gate parasitics as well as the harmful couplings between the gate and the other nodes [3.18]. In the simulation, the output stage can generate a saturated output power of 26.5-dBm to the 50- $\Omega$  load at 10-GHz.

The impedance matching formulas in (2.1) were also applied to design the driving stage as well as the input PS. Intuitively, the inter-stage TF size was designed such that its secondary inductance resonates out the gate capacitance of the output transistor. To give freedom in choosing the device size of the driving stage, a capacitor  $C_2$  was employed to tune the capacitance at the input side. The device size of the driving stage was chosen in consideration of the linearity, the gain, and the power efficiency of the PA. The driving active device should be large enough to drive the power stage into the saturation region before its output power is compressed. Besides, a relatively large driving amplifier consumes a large DC power which degrades the overall power efficiency. Considering those issues, a suitable transistor size of 160- $\mu\text{m}$  was chosen for the driving stage, resulting in a simulated output 1-dB gain compression point (OP1dB) of 23.5-dBm at 10-GHz for the whole PA. The signal level processed by the input PS is small, thereby its efficiency is negligible to the whole PA design. Instead, the impedance matching for the input side is more problematic due to a relatively high impedance of the input gates. To enhance the impedance matching capability, low-quality MOS capacitors were shunted to the gate of the driving transistor to degrade the Q-factor of the resonator at the gates as well as to reduce the size of the input PS. Moreover, a pair of capacitors including  $C_{i1}$  and  $C_{i2}$  was used to transfer a relatively high input impedance seen from the PC to the 50-ohm source. To characterize the PA accurately, the whole physical layout of the PA was modeled in the EM simulation (HFSS). The 3-D structure of the proposed PA is illustrated in Figure 3.8. The PA was fabricated on 65-nm CMOS, and an image of the chip is shown in Figure 3.9. The chip size of the full PA including all DC and RF pads is  $1 \times 0.9 \text{ mm}^2$ , and the core size is  $0.6 \times 0.57 \text{ mm}^2$ .

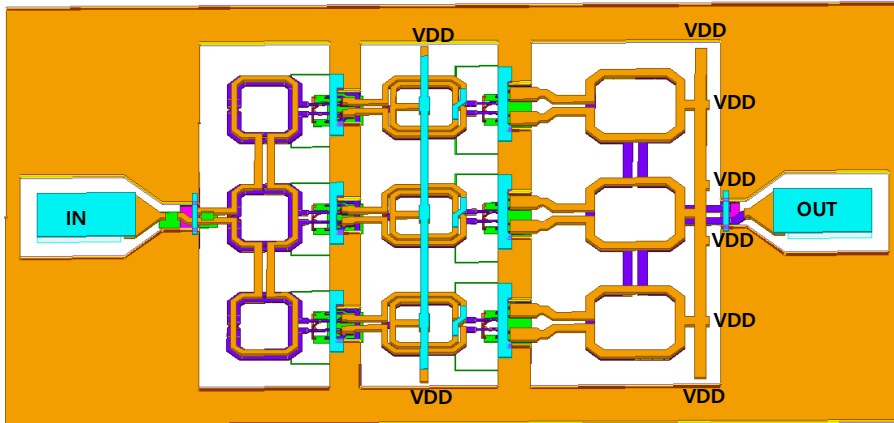


Figure 3.8. 3D HFSS physical structure of the whole PA.

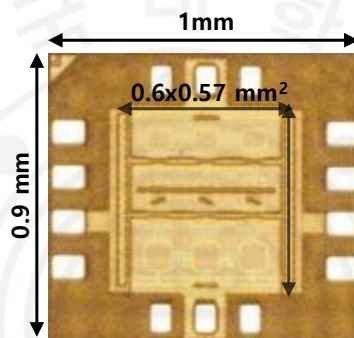


Figure 3.9. Photograph of the fully integrated X-band 6-way power combining PA chip.

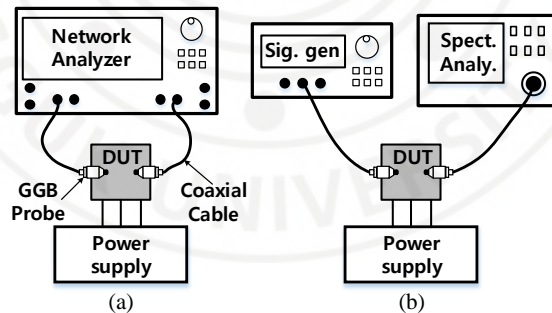


Figure 3.10. Measurement setups of the S-parameters (a) and large-signal merits (b).

### 3.2.5 Measurement results

Figure 3.10 illustrates measurement setups of S-parameters and large-signal metrics of the X-band PA. In measurements, the PA consumed 865 mA of DC quiescent current at 1.2-V with no applied RF input. The S-parameters were measured using a vector network analyzer (VNA) Keysight N5224A (10 MHz to 43.5 GHz) and an on-wafer probe station. RF probes for the measurement and the cable connections were calibrated using a CS-5

substrate. A comparison of the simulated and measured S-parameters of the PA is shown in Figure 11. Both measurements and simulation results are in agreement. A peak gain of 25.9-dB is observed at 9.5-GHz, with a bandwidth of 2-GHz recorded between 8.7-GHz and 10.7-GHz. In general, the measured  $S_{11}$  and  $S_{22}$  results are superior to those from simulations. At the load, we measured a minimum  $S_{22}$  of about -40 dB at a very high impedance matching level. In terms of impedance matching, this further substantiates the advantages of the VCT over the CCT. The isolation between the outputs and the input, i.e.,  $S_{12}$ , was measured to be smaller than -50 dB.

The PA was measured with a signal generator Agilent 83623B (10-MHz-20-GHz) and a spectrum analyzer Agilent E4407B (9-kHz-26.5-GHz). As depicted in Figure 12, the simulation and measurement performances of the PA based on input power,  $P_{sat}$ , power gain, and PAE are shown. The measured power gain and  $P_{out}$  profiles are quite similar to those found in the simulation results proving that the PA is linear. In the case of small input signals, the measured PAE matches the simulation results almost exactly. PAE, however, degrades when the signal becomes larger in measurement, which illustrates the limitations of the transistor model in the large signal domain.

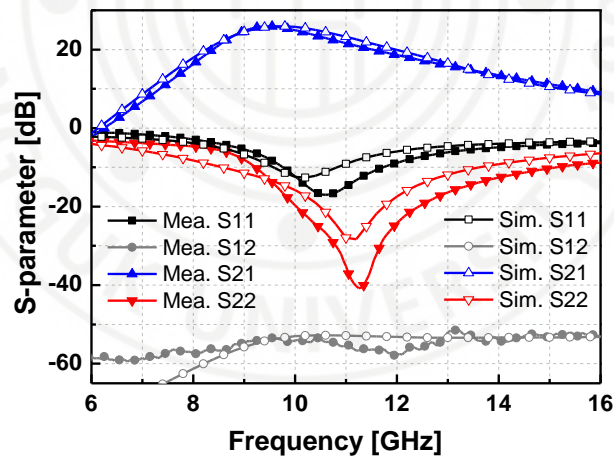


Figure 3.11. Simulated and measured S-parameters of the 6-way PA.

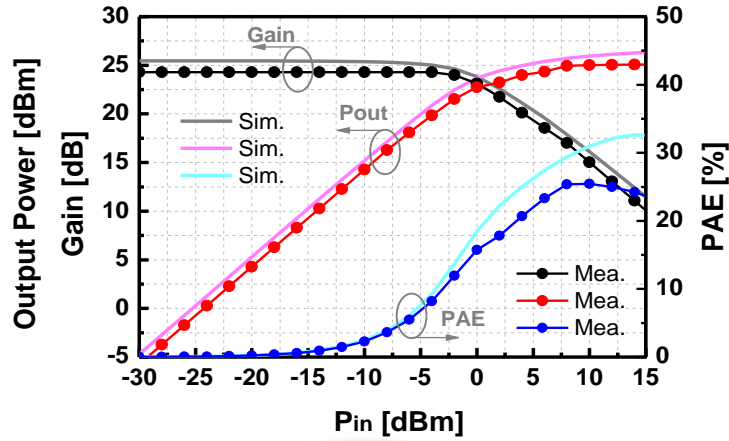


Figure 3.12. Simulated and measured output power ( $P_{out}$ ), Gain, and power-added efficiency (PAE) versus input power ( $P_{in}$ ) of the PA at 10-GHz.

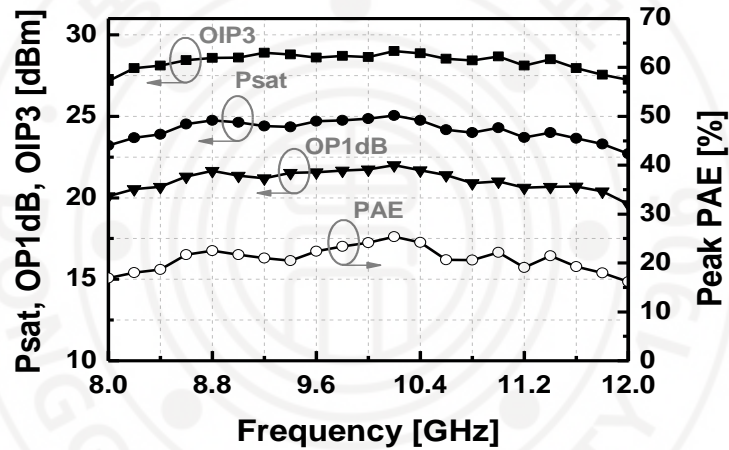


Figure 3.13. Measured  $P_{sat}$ , OP1dB, OIP3, and peak PAE of the 6-way PA in the X-band.

The PA's large-signal performance was measured in the whole X-band with 0.2-GHz frequency steps. To measure the output third-order interception point (OIP3), we applied two tones with a spacing of 20 MHz. Figure 3.13 displays the results of the  $P_{sat}$ , OP1dB, OIP3, and peak PAE measurements. PA achieves a maximum  $P_{sat}$  of 25.1 dBm at 10.2-GHz, and a peak PAE of 25.4% is obtained at the same frequency. OP1dB was 22-dBm, and OIP3 was 29 dBm for the PA at 10.2-GHz. The measured  $P_{sat}$  varied less than 1 dB between 8.4 GHz and 11.4 GHz. Across the whole X-band, the measured  $P_{sat}$  is greater than 22.7-dBm, the measured OP1dB is higher than 19.6-dBm, and the peak PAE is greater than 16.1%.

In Table 3.2, the PA is compared with other silicon-based PAs that have recently been reported around the X-band. As a result of its overall-high performance, the PA achieves the highest FoM for CMOS PAs and is even better than PAs designed in SiGe.

Table 3.2. Summary of State-Of-Art Silicon-based PAs around X-band

Ref.	Tech. (CMOS)	Combining Topology	Freq. (GHz)	V <sub>DD</sub> /V <sub>CC</sub> (V)	P <sub>sat</sub> (dBm)	Gain (dB)	Peak PAE (%)	OP1dB (dBm)	Area (mm <sup>2</sup> )	DC-Diss. [mW]	FoM
<b>This</b>	<b>65-nm CMOS</b>	<b>VCT6</b>	<b>8.7-10.7@10</b>	<b>1.2</b>	<b>25.1</b>	<b>25.9</b>	<b>25.4</b>	<b>22.0</b>	<b>0.9x1.057x0.6*</b>	<b>1038</b>	<b>85.0</b>
[3.16]	90-nm CMOS	VCT2	5.2-13@8	2.8	25.2	18.5	21.6	22.6	0.7	NA	75.1
[3.17]	180-nm CMOS	VCT2-CCT3	7-10@9	3.3	27.1	11.2	22.7	24.2	0.88	1267	70.9
[3.18]	180-nm CMOS	VCT2	6.5-13@9.5	3.6	21.5	25.3	20.3	20.2	0.63	713	79.4
[3.19]	45-nm SOI	Stacked	9-15@12	4.8	22.8	9.8	21.8	21.9	0.22	NA	66.0
[3.20]	180-nm CMOS	VCT4	8.6-10.3@9.5	3.0	24.5	25	18	NA	1.2	960	81.6
[3.21]	180-nm CMOS	CCT2	7-12@10	3.6	23.8	14.5	25.8	17.6	0.47	691	72.4
[3.22]	65-nm CMOS	VCT2	8-11.4@9.5	1.2	20.5	24.4	24.5	15.2	0.48	347	78.3
[3.23]	180-nm CMOS	CCT2	7.4-8.3@8	1.8	18	19.2	22.6	14.9	0.43	NA	68.8
[3.24]	180-nm CMOS	CCT4-VCT2	10-12@11	5	29.6	11	15.5	28.2	2.1	4060	73.3
[3.25]	65-nm CMOS	VCT2	10	1.8	21.4	NA	33.3	21	NA	614	NA
[3.31]	130-nm SiGe	2-way CCT	8.6-11.2@10**	3	26.5	16.1	53.4	NA	0.81	15.6	79.9
[3.32]	180-nm SiGe	2-way VCT	7.2-10.2@10**	3.5	27	21	36	NA	0.95	578	83.5
[3.33]	130-nm SiGe	2-way CCT	8-12@10**	7.5	29.5	27.7	17.8	28.2 <sup>#</sup>	2.66	NA	89.7
[3.34]	350-nm SiGe	2-way VCT	11-13@12	1.8	23.4	21.2	37.3	20.4	1.71	NA	81.9

$$FOM = P_{sat} \text{ (dBm)} + Gain \text{ (dB)} + 10 \log (PAE [\%] \times f^2 \text{ [GHz]})$$

\* PA core only; # Estimated from figure

\*\* BW is defined as the frequency range of the power gain 1 dB lower than that at 10 GHz

### 3.3 Power amplifier design using 1:2 output transformer

#### 3.3.1 Power amplifier design

The X-band push-pull PA schematic is shown in Figure 3.14. This PA has a driving stage and power stage, as well as matching networks at the input, output, and inter-stage



levels. Each transformer is equipped with a primary capacitor, a secondary capacitor, or both at its two ends for resonance with the corresponding inductors. In the PA design, the output matching network plays a very pivotal role since it must deliver ample power to the load. Through the use of a 1:*n* transformer for output matching, the output matching network is also capable of performing impedance transformation, therefore reducing the load impedance of the transistor. Consequently, a high output power can be delivered under a relatively low supply voltage environment since more current can be drawn by the transistor [3.35].

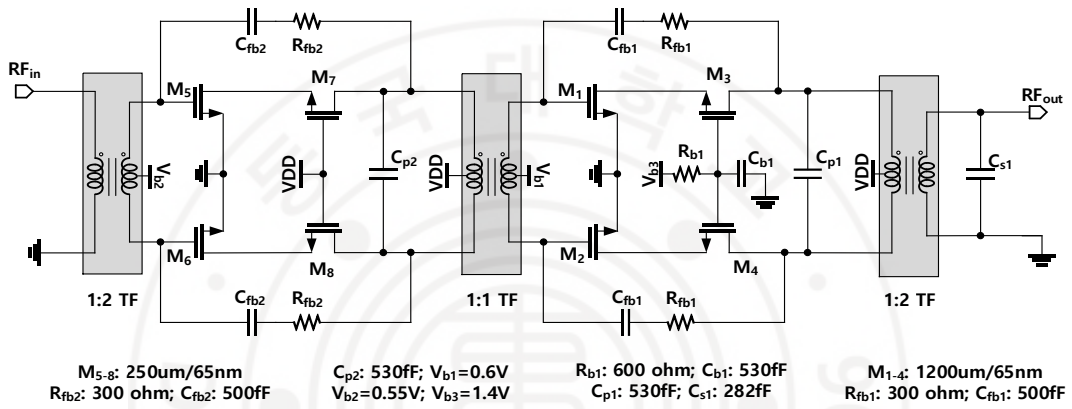


Figure 3.14. A schematic of the two-stage TF-coupled PA.

In the PA, MOS devices can be viewed as switches. Conductance can therefore be used to assess the switching device's ability to draw current from the load in generating output power. Accordingly, we can define a quantity known as effective conductivity (EC) as follows:

$$G_s = \frac{P_{out}}{V_{sup}^2}, \quad (3.3)$$

where  $P_{out}$  is the output power delivered to the load and  $V_{sup}$  stands for the supply voltage.  $G_s$  are dependent on both the output matching network and the cascode device. Optimal output transformers are therefore crucial in a successful PA design.

As a common device in CMOS PAs, a cascode boosts gain and improves stability in the RF circuits [3.36]-[3.38]. When the drain-bulk junction  $D_{jdb}$  (shown in Figure 3.15b) is connected to the ground, the voltage swing of the drain is limited by the breakdown voltage at the drain-bulk junction in bulk-CMOS technology. As a result, the cascode device ( $M_1$ )

is typically implemented with a thick-oxide transistor with a high breakdown voltage [3.18]. Although the cascade device's channel resistance ( $R_{on}$ ) is increased due to the thick-oxide MOS's longer channel length, the increased effective conductivity  $G_s$  limits the device's current driving capability. Cascode's gain is also significantly reduced by the body effect.

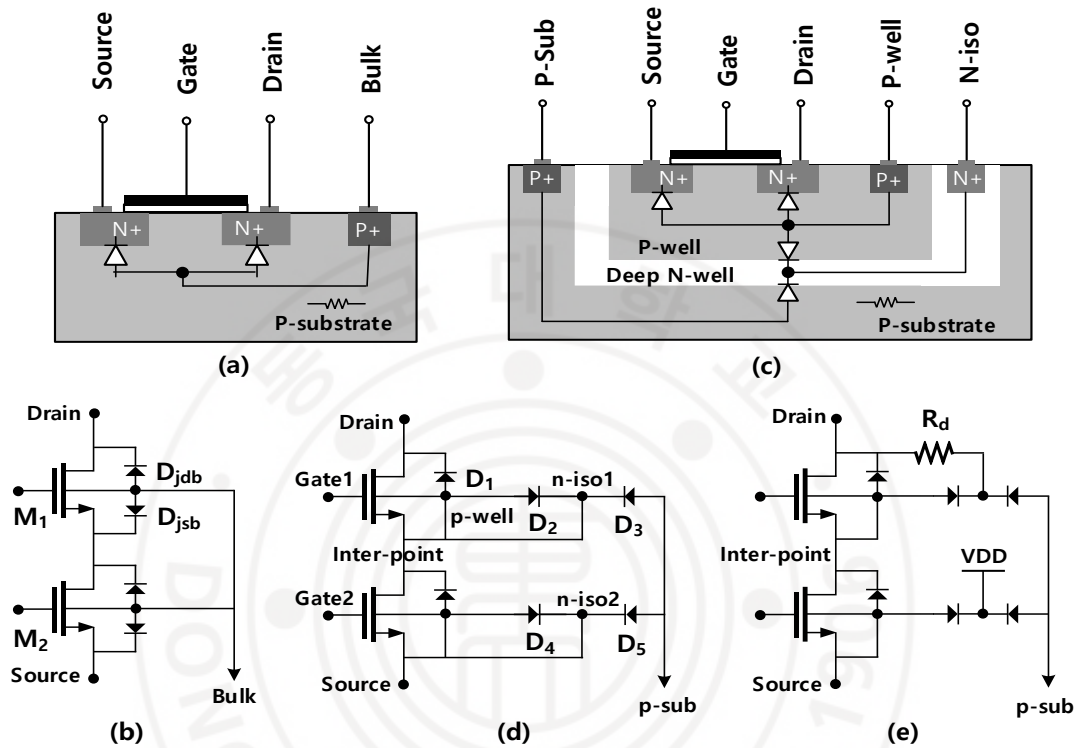


Figure 3.15. Cascade structure of NMOS (a) The structure of the bulk CMOS, (b) NMOS cascode using bulk CMOS, (c) the structure of the triple-well CMOS, (d) conventional cascode of triple-well CMOS, and (e) the triple-well CMOS cascode using a biasing resistor ( $R_b$ ).

In order to overcome the limitation of bulk-CMOS technology, a cascode of triple-well transistors can be used, as illustrated in Figure 3.15d, where the body effect is avoided by tying the source of each transistor to its p-well as shown in [3.36]. Because of the stacked configuration, the voltage swing at the inter-point  $V_{ip}$  is halved compared to the drain voltage ( $V_{drain}$ ), reducing the stress on the junction diodes of the cascode structure significantly. As shown in Figure 3.15d, each p-well is connected to its  $n-iso$  which can deteriorate the isolation between  $p-wells$  and  $p-sub$  of  $M_{1-2}$ . To improve these isolations, a resistor  $R_d$  can be utilized to bias for the  $n-iso$  of the cascode transistor ( $n-iso1$ ) from its drain. The other  $n-iso$  node of the main transistor ( $n-iso2$ ) can be tied to the supplier as shown in Figure 3.15e.

The resistance of the  $n$ -iso1 node and its  $p$ - $n$  junction capacitances determine the voltage at the  $n$ -iso1 node  $V_{n\text{-iso1}}$ . In order to avoid breakdown voltage of diode  $D3$ ,  $R_d$  must be chosen such that  $V_{n\text{-iso1}}$  is higher than the  $p$ -well node, but low enough to avoid a rise in  $V_{n\text{-iso1}}$ . RC bias circuits similar to those used in SOI-CMOS technology [3.36] are employed to bias the gate of M1 in order to achieve an equal voltage distribution over both NMOS devices in the cascode configuration. Figure 3.16a shows the voltages of the nodes presented in Figure 3.15e when  $P_{\text{out}} = 21.5$  dBm at 11 GHz. It can be seen that the peak drain voltage  $V_d$  almost doubles that of the inter-point voltage  $V_i$ , while the voltage of the  $n$ -iso1 node  $V_n$  is remained higher than  $V_i$  by nearly 0.3 V. With a gate voltage swinging around 1.4 V, the gate-to-source and drain-to-gate voltages remain within the safe range. In Figure 3.16b, the PAE of PA is compared when two different configurations in Figure 3.16d and Figure 3.15e are used. Compared to the PA without  $R_b$  (Figure 3.15d), the PA with the triple-well cascode device biased with  $R_d$  (Figure 3.15e) achieves a higher PAE.

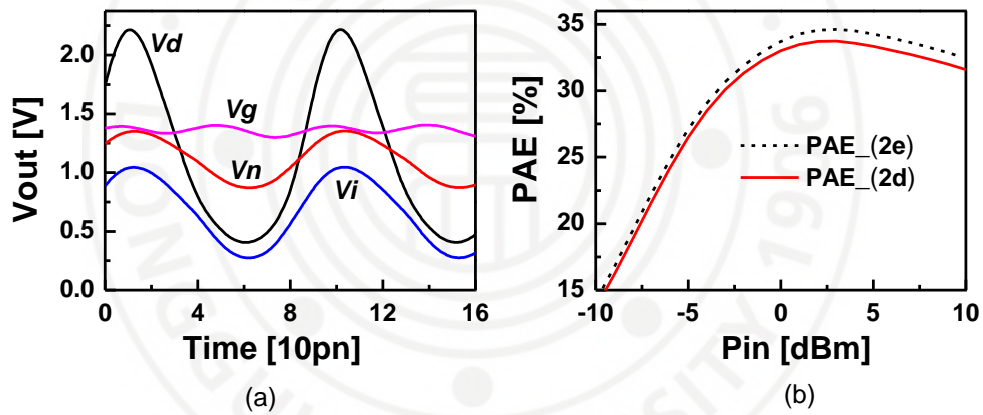


Figure 3.16. (a) The simulated voltage waveforms of the nodes in Figure 3.15e: the drain ( $V_d$ ),  $n$ -iso1 ( $V_n$ ), gate1 ( $V_g$ ), and inter-point ( $V_i$ ). (b) The power-added efficiency of the PA when using the configurations in Figure 3.15d ( $\text{PAE}_{2d}$ ) and Figure 3.15e ( $\text{PAE}_{2e}$ ).

We introduce an RC feedback network in the designed PA to make the PA more stable and to increase bandwidth. We conducted a transient analysis in the time domain and a k-stability test in the frequency domain to ensure that the PA is stable during its operation. Figure 3.14 shows the circuit elements and biases of the PA. The X-band CMOS PA was fabricated for verification. Figure 3.17 shows a pictorial representation of the chip.

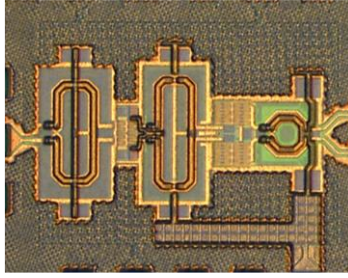


Figure 3.17. A microphotograph of the CMOS PA using 1:2 output TF.

### 3.3.2 Measurement results

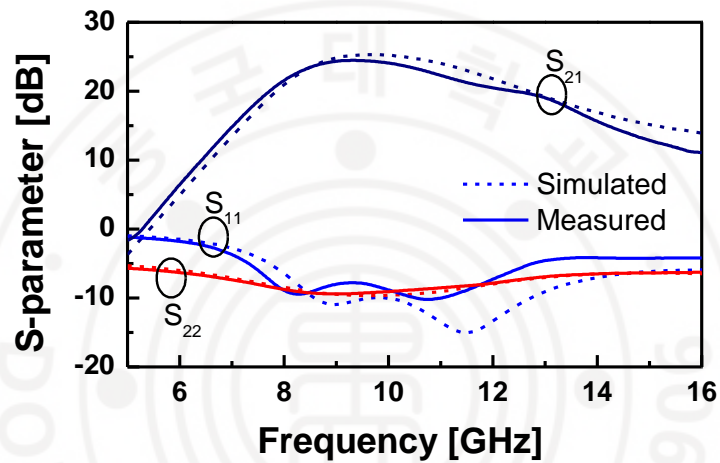


Figure 3.18. Measured s-parameters the X-band PA using 1:2 TF.

DC current consumption by the X-band PA is 289 mA when the input power is 0 dBm at 10 GHz; the DC current consumed varies with input power and operating frequency. Figure 3.18 illustrates the measured S-parameters. A graph of the gain, output power, and PAE of the PA versus input power in the range of 8-11 GHz is shown in Figure 3.19. Figure 3.20 presents graphs of the simulated and measured saturated power output ( $P_{\text{sat}}$ ), output 1-dB gain compression point (OP1-dB), and peak PAE from 8-11 GHz. It also shows the measured OIP3 of the PA. Compared with the simulation, the measured performance of the PA was degraded more at a higher frequency regime since the center frequency was shifted to the lower region. PAE degraded by about 10% at 11GHz. In the implemented PA, the on-chip transformer had a reduced Q value, which resulted in a frequency shift caused by the inaccuracy in parasitic extraction. In Table 3.3, we compare the performance of CMOS PAs (including SOI-CMOS) around the X-band reported recently.

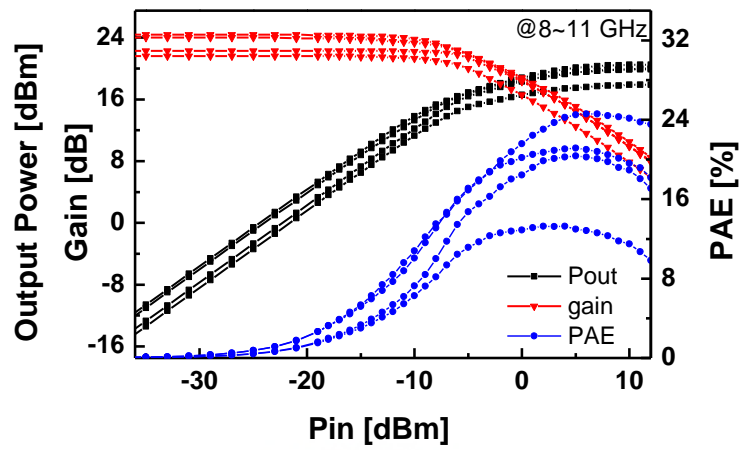


Figure 3.19. Measured output power of the PA at different frequencies.

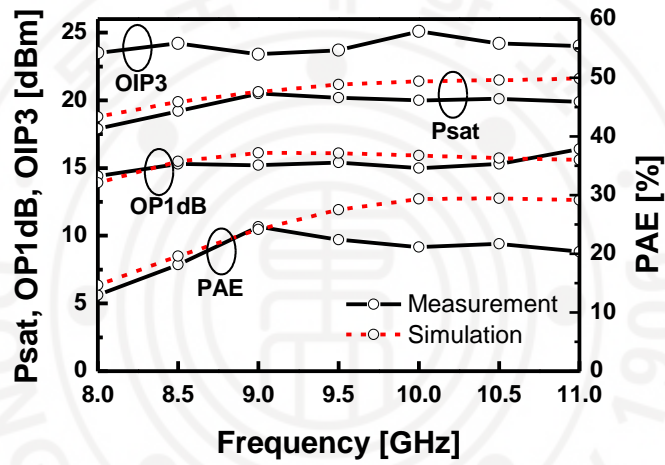


Figure 3.20. The measured and simulated  $P_{sat}$ ,  $OP_{1dB}$ , peak PAE, and measured  $OIP_3$  versus frequency.

Table 3.3. Comparison of CMOS PAs around the X-band

Reference	[3.16]	[3.17]	[3.18]	[3.19]	[3.21]	[3.20]	<b>This work</b>
Process	90-nm CMOS	0.18-um CMOS	0.18-um CMOS	45-nm SOI-CMOS	0.18-um CMOS	0.18-um CMOS	<b>65-nm CMOS</b>
Frequency (GHz)	5.2-13@8	7-10@9	6.5-13@9.5	9-15	7-12	8.6-10.3	<b>8-11.4@9</b>
$P_{\text{sat}}$ (dBm)	25.2	27.1	21.5	22.8	23.8	24.5	<b>20.5</b>
OP1dB	22.6	24.2	20.2	21.9	17.6	N/A	<b>15.2</b>
Gain (dB)	~19	11.2	25.3	9.8	14.5	25	<b>24.4</b>
Peak PAE (%)	21.6	22.7	20.3	21.8	25.8	18	<b>24.5</b>
VDD	2.8	3.3	3.6	4.8	3.6	3.0	<b>1.2</b>
Area (mm <sup>2</sup> )	0.70	0.88	0.63	0.22	0.47	1.2	<b>0.48</b>
$EC (P_{\text{sat}}/V_{\text{sup}}^2)$ (S)	42.2	47.1	10.9	8.3	18.5	31.3	<b>77.9</b>

### 3.4 Single-pull class A/B power amplifier design

#### 3.4.1 Design the Two-Stage Single-Pull Power Amplifier

The circuit schematic diagram of the designed two-stage PA with the physical layout of the output power combiner is given in Figure 3.21. The driving amplifier at the first stage is the single-pull CS amplifier with a transformer at the output while the second stage is the combination of the two similar structures.

The transformer-based on-chip power combiner (PC) was “figure-8” shaped and implemented by the top-most aluminum metal layer with a thickness of 2 $\mu\text{m}$ . With this configuration at the output, we chose the optimal size of the transformer corresponding to the size of the active device to achieve a simple output matching network. At 8 GHz, the EM simulation of the PC shows that it has two primary inductors of 240 pH, a secondary inductor of 650 pH, and two coupling factors of 0.79. The quality factors of the two primary coils are 11.5 while that of the secondary winding is 7.5. An additional capacitor ( $C_{p1}$  and  $C_{p2}$ ) is applied to the drain node to resonate out the primary coil inductance of the power combiner to reduce the size of the required inductance of the primary coil. The two resonating capacitors are connected to  $V_{\text{DD}}$  instead of the ground to facilitate layout.



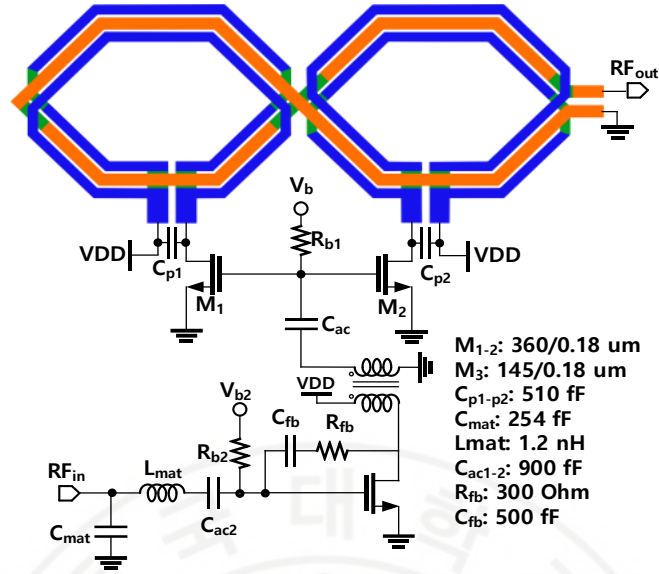


Figure 3.21. Schematic circuit of the two-stage single-pull power amplifier on 180-nm CMOS.

In both stages, an AC capacitor ( $C_{ac1}$  and  $C_{ac2}$ ) was used to separate DC bias from the AC signal path. The output of the driving stage was connected to the gates of the power stage via  $C_{ac1}$  which may include only a small resistance at X-band which could make the PA less stable. To cope with this issue, we exploited a shunt RC feedback network which consists of a capacitor  $C_{fb}$  in series with a resistor  $R_{fb}$  connect from the drain to the gate of the MOS. It helps to withstand the gain compression of the driving stage, makes the PA more stable, and increases the bandwidth. Figure 3.22 illustrates the output voltage waveform when  $V_{DD}$  is excited by a step function while Figure 3.23 depicts the parameter  $S_{21}$  in the case with and without the shunt RC feedback. It took around 1 ns for the output voltage swing to turn off when using the shunt RC feedback, a twice time faster than the case without the RC feedback network which required approximately 2 ns. On the other hand, the gain of the PA was degraded.

The RF input impedance of the single-pull input stage is matched with an L-matching network consisting of  $L_{\text{mat}}$  and  $C_{\text{mat}}$ . Since the parasitic inductance in the bias paths can degrade the stability of the PA, bias resistors ( $R_{b1}$  and  $R_{b2}$ ) were used for de-Qing the line inductances. All the component values are given in Figure 3. The fabricated PA has the size of  $0.83\text{mm} \times 0.52\text{mm}^2$  excluding the pads, and a photograph of the chip is presented in Figure 3.24.

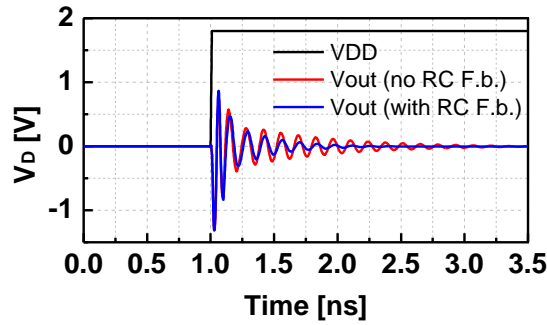


Figure 3.22. The output waveform of the PA when the VDD is turned on at  $1\text{ ns}$  in the case with and without the shunt RC feedback.

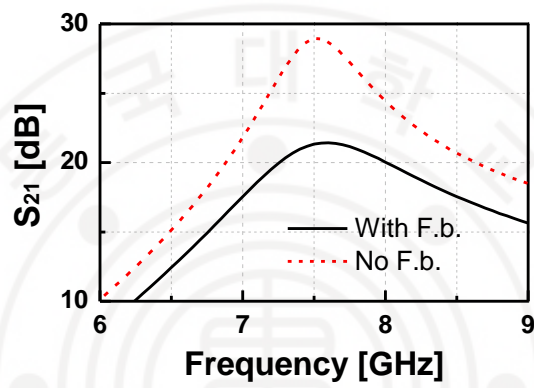


Figure 3.23. The gain ( $S_{21}$ ) of the PA in the case with and without the shunt RC feedback.

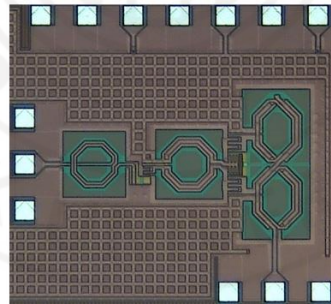


Figure 3.24. The microphotograph of the fabricated two-stage PA on a 180-nm CMOS process (full chip size is  $0.83\text{ mm} \times 0.52\text{ mm}$ ).

#### 3.4.2 Measurement results

Figure 3.25 compares the simulated and measured S-parameters of the implemented PA. It shows around 0.4-GHz of frequency down-shift and a 1.6-dB of gain degradation compared with simulation results. The simulated and measured power performances of the PA are given in Figure 3.26. The implemented two-stage PA has measured 3dB-bandwidth of 0.9 GHz ranging from 7.4-8.3 GHz which corresponds with the simulation result. The measured

peak power added efficiency (PAE) is 22.6% at  $P_{in} = 5$  dBm and has a relatively flat response concerning the input power. The output 1-dB gain compression point (OP1dB) was 15 dBm. The output third-order intercept point (OIP3) was measured to be 23.5 dBm with a 20 MHz frequency offset at 8 GHz. The implemented PA obtained the saturated output power ( $P_{sat}$ ) of 18 dBm. A comparison of the implemented PA with other recently reported X-band PAs in CMOS is given in Table 3.4. While having the smallest area among bulk-CMOS PAs and operating with a low-voltage supply (1.8 V), the proposed two-stage PA shows a comparable PAE among others.

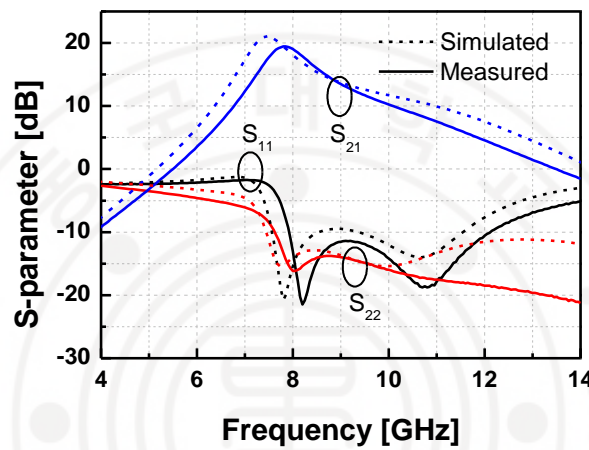


Figure 3.25. Simulated and measured S-parameters of the single-pull PA.

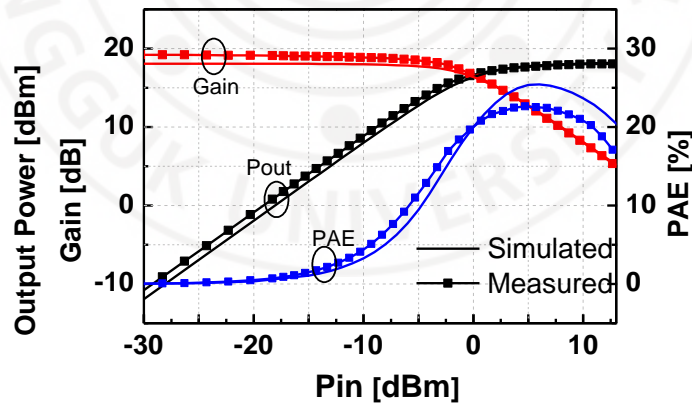


Figure 3.26. The simulated and measured power performance of the PA at 8GHz.

Table 3.4 Summary of the CMOS PAs around X-band

Ref.	[3.16]	[3.18]	[3.19]	[3.17]	[3.20]	<b>This work</b>
Process	90nm CMOS	0.18um CMOS	45nm CMOS SOI	0.18-um CMOS	0.18um CMOS	<b>180um CMOS</b>
Freq. (GHz)	5.2-13@8	6.5-13@9.5	9-15	7-10@9	8.6-10.3	<b>7.4-8.3@8</b>

Psat (dBm)	25.2	21.5	22.8	27.1	24.5	<b>18</b>
OP1dB	22.6	20.2	21.9	24.2	N/A	<b>14.9</b>
Gain(dB)	~19	25.3	9.8	11.2	25	<b>19.2</b>
Peak PAE(%)	21.6	20.3	21.8	22.7	18	<b>22.6</b>
V <sub>DD</sub>	2.8	3.6	4.8	3.3	3.0	<b>1.8</b>
Area (mm <sup>2</sup> )	0.70	0.63	0.22	0.88	1.2	<b>0.43</b>

### 3.5 Reference

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## IV. E-band Transformer-coupled Power Amplifiers

### 4.1 Introduction

Recently, a wide variety of research efforts in millimeter-wave transceivers has been carried out toward their use in wideband wireless applications [4.1]-[4.8]. The growing demand for a 5G backhaul solution has necessitated the development of an efficient millimeter-wave line-of-sight (LOS) wireless communication link system for the E-band [4.9]. Moreover, W-band is suitable for use in radar sensors for traffic vehicles. As a result of the small wavelength, radar sensors can detect small objects such as people, small cars, and traffic poles with more precision. High-frequency sensors are also able to capture higher velocity, which is essential for collision-avoidance systems [4.10]. The second advantage of W-band radars is their superior reliability in extreme conditions (e.g., heavy rain, dense fog, snow) [4.11]. This is because electromagnetic waves at high frequencies have strong penetration properties. ITU, therefore, recommended a band of 76-81 GHz for automotive radar applications.

When it comes to full implementations of radar sensors for use in the W-band, CMOS technology is preferred as it can provide adequate power and efficiency with its low cost and high integration capability. Low breakdown voltages of CMOS make it difficult to design high-performance PAs with such high frequencies. Furthermore, millimeter-wave circuits suffer from lossy substrate environments for passive devices in addition to a lower power gain for active devices.

For a typical channel with a radar cross-section (RCS) of a mid-car ( $30\text{-m}^2$ ), 13-dBm of power is required for the transmitter to cover the standard detection distance of 250 meters [4.12]. However, for a reliable operation, a PA with a high output power is preferable. The casual condition could also be ideal for using lower than saturated output power, while adverse conditions could require peak power.

With a CMOS PA, it is now possible to achieve an output power greater than 13-dBm without the use of a more complex power combining network, which could degrade the power efficiency because of the power combiners' extra losses at the output [4.13]-[4.14]. Consequently, it is natural to use the PA without a complex combiner/splitter to obtain benefits in efficiency and occupancy with less design effort [4.11]. Choosing the largest size of an active device at the output stage is essential for maximizing the power of a single-way PA while maintaining impedance matching with surrounding circuits. To achieve the

highest possible output power with minimal occupied space, the size of the active device must be optimized.

In section 4.2, we demonstrate an automotive radar application using a transformer-based push-pull PA with ultra-thick metal (UTM) of copper at 77 GHz for 65 nm CMOS. The push-pull amplifier consists of three stages and is designed to have a gain exceeding 20 dB and a power output exceeding 13 dBm. An emphasis is placed on the design procedure in selecting a high-efficiency mm-wave PA with an optimal device and proper transformer (TF) sizing.

Multiple transistors can be stacked to sustain a higher voltage supply at the output of a CMOS PA, which boosts the output power. There is, however, a limit on the number of transistors that can be used because of the breakdown voltage at the drain-body junction. In light of this limitation, silicon-on-insulator (SOI) CMOS processes are preferred due to the physical isolation of the floating body, which stimulates the use of an SOI FET-stacked PA structure to increase performance [4.15-4.18]. Multi-transistor stacks tend to degrade the overall linearity of the active devices, resulting in a lower compression point (OP1dB) for the PA [4.15], [4.16]. In addition, SOI CMOS is more expensive than bulk CMOS, which limits availability and foundry access.

When increasing the power output of a PA, power combining is one of the more common technologies. In power combining, two common techniques are employed: current power combining (CPC) and voltage power combining (VPC) [4.15]-[4.32]. In passive devices, the CPC technique is typically applied to improve current handling capabilities and reduce the overall effective inductance [4.19], [4.33]. When the device width increases, the MOS performance typically degrades [4.23]. The reason for this is that when laying out a larger transistor, one must use extra electrical connections involving bottom metal layers, which have a high conductor loss. Parallel-connected transistors can handle a larger current than a single large transistor when the current is split between several transistors [4.33]. The performance of one small inductor is typically lower than that of two inductors of the same inductance connected in parallel. To optimally drive the load, the CPC technique does not offer any advantages for active device sizing since the size of the device must be reduced by  $1/n$  times. As opposed to this, VPC techniques enlarge devices by  $n$  times through the use of a multi-way combination scheme as presented in chapter 3.2 [4.34].

When the number of combinations increases in a transformer-based VPC technique, the secondary coil has to be longer than the primary one to allow for magnetic coupling.

Consequently, it results in a lower self-resonance frequency (SRF) for the realized combiner. According to conventional wisdom, a power combiner (PC) or power splitter (PS) should operate below its SRF to avoid any ambiguity in the mode of operation as well as any difficulties with impedance matching. Other than the push-pull PA structure, which is intrinsically a two-way VPC, higher-order VPC implementations are not popular in the literature for E-band. A notable exception is found in [4.30] and [4.31], where the authors presented a PA structure based on a four-way VPC technique based on the concept of the distributed active transformer (DAT) in [4.35]. Similarly, an 8-way VPC was implemented at 78 GHz based on the same concept [4.32]. When the differential pairs of transistors are neutralized by capacitance neutralization, the symmetrical layout of the input signal paths is more challenging when distributed VPC is employed [4.36].

Section 4.3 describes an 8-way PA with power combining/splitting techniques in both the voltage and current domains. Mixed combining allows for a more flexible realization of the PC/PS structure than DAT combiners because its input and output ports are fed in a single direction. Furthermore, this layout structure can easily be extended to achieve a higher level of VPC. Despite this, the longer secondary coil route reduces the SRF of the PC significantly. As such, it is natural for a PC to operate beyond its SRF and to face the issue of impedance matching at high frequencies. Using a combination of voltage and current analysis, we explore the feasibility of operating a voltage PC beyond its SRF. In order to identify the frequency bands where a PC/PS can work efficiently, a simplified method employing an equivalent two-port network (E2PN) was developed. Using the E2PN, we can assess how voltage imbalance between input ports in a 2-way PC affects the power efficiency used to determine the impedance match in the network.

In section 4.4, we demonstrate the use of inductive unilaterization for a push-pull power amplifier to achieve a well-balanced overall PA performance. Using a transformer-based push-pull configuration and an inductive shunt-shunt feedback scheme in 65-nm CMOS technology, the proposed PA obtained a PAE of 14.1% and saturated output power ( $P_{\text{sat}}$ ) of 16.3 dBm. A compact inter-stage conjugate matching was implemented using stacked TFs, resulting in a small and efficient PA. The PA achieved a high power gain (28.1 dB) with a minimal core area of 0.121 mm<sup>2</sup>.

## **4.2 Compact and high-efficiency power amplifier design in 77-GHz**

#### 4.2.1 Power amplifier design

The simplified schematic of the proposed PA is presented in Figure 4.1. It consists of three stages of the push-pull amplifier, including the input stage, driving stage, and output stage. Besides various advantages in a compact size and power delivery, the transformer also provides galvanic isolation and electrostatic discharge (ESD) protection at the input and output ports.

In each amplifying stage, neutralization capacitors are included to improve the stability factor, which eventually results in better impedance matching. This architecture also increases the isolation between input and output and the gain of each push-pull amplifier stage. In this design, metal-oxide-metal (MOM) capacitors were used to achieve a high-precision embedding network instead of using more compact MOS capacitors with a lower Q-factor [4.14]. The value of the neutralization capacitor is chosen to be roughly  $C_{gd}$  of the transistor [4.36]. Specifically, Rollet's stability factor ( $K-\Delta$ ) and the maximum stable gain ( $G_{ma}$ ) values of the amplifier were investigated carefully to ensure its stable operation as we did for the X-band power amplifier design [4.34].

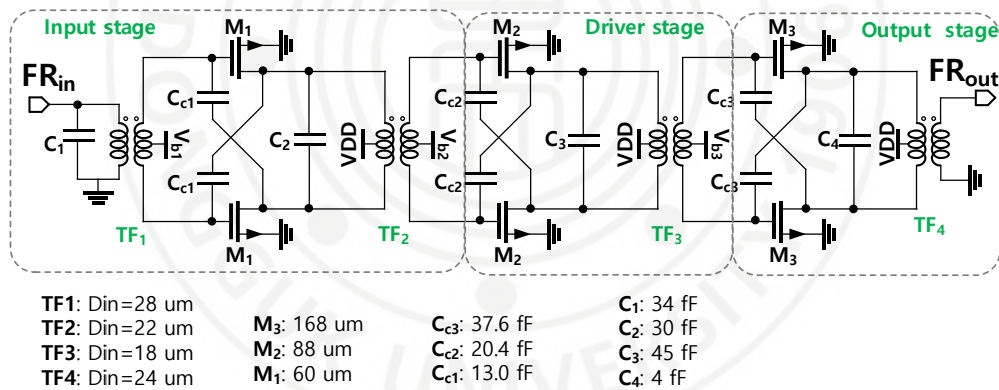


Figure 4.1. Schematic of the 77-GHz PA.

The gate bias voltage ( $V_{GS}$ ) for the three stages was chosen considering the trade-offs between the dc-power dissipation and the maximum output power. The  $V_{GS}$  for the output stage (3<sup>rd</sup>) was chosen to be 0.7 V to achieve a good output power while the  $V_{GS}$  for the input and the driving stages was chosen to be 0.6 V for a better power gain [4.34]. The inter-stage impedance matchings using a transformer were performed with the assistance of the analysis in chapter 2. In the following, we consider several angles when designing the PA.

a) *The significance of matching network loss depending on the gain*

Let us consider a PA with the gain stage having matching input and output networks, as presented in Figure 4.2. The gain stage has a transducer power gain of  $G_T (= G_{ma} - IL_{Min} - IL_{Mout})$  with well-matched input/output ports by assuming that  $G_{ma}$  is the maximum available gain from an unconditionally stable device with input and output matching networks (TMN<sub>in</sub> and TMN<sub>out</sub>, respectively) that provide good enough impedance matching with  $IL_{Min}$  and  $IL_{Mout}$ , respectively. The effect of TMN<sub>in</sub> and TMN<sub>out</sub> is quite different in the whole PA performance.

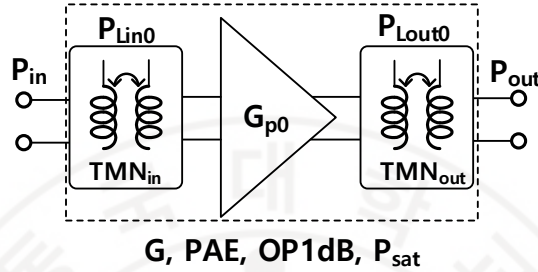


Figure 4.2. An amplifier with input and output matching networks.

Let us evaluate their effect by assuming that either the insertion loss of TMN<sub>in</sub> or TMN<sub>out</sub> increases by 1 dB. Since the PAE needs to be compared at the same output power level for a fair comparison, we maintain the whole gain level as constant. Thus, to keep the same output power, if  $IL_{Min}$  is increased by 1 dB, then  $P_{in}$  should be increased by 1 dB accordingly. Therefore, the new PAE ( $PAE_{pk(new)}$ ) affected by the variation in power gain  $\Delta G_{TdB}$  from the TMNs can be calculated as

$$r_{PAE} = \frac{PAE_{pk(new)}}{PAE_{pk}} = \frac{P_{out} - 10^{-\Delta G_{TdB}/10} \times P_{in}}{P_{out} - P_{in}} = \frac{G_T - 10^{-\Delta G_{TdB}/10}}{G_T - 1} \quad (4.1)$$

From (4.1), the effect of  $IL_{Min}$  on the PAE is quite minor when  $G_T$  is relatively large. If  $G_T$  is reduced from  $G_{TdB} = 20$  to 19 dB (i.e.,  $\Delta G_{TdB} = -1$  dB) due to the increase in  $IL_{Min}$ , the calculated  $r_{PAE}$  is merely 0.997 while  $r_{PAE} = 0.88$  for the PA with  $G_{TdB} = 5$  dB with the same degradation in TMN<sub>in</sub> ( $\Delta G_{TdB} = -1$  dB). It can be seen that the influence of TMN<sub>out</sub> on PAE is more direct and stronger than that of TMN<sub>in</sub>. Thus, the influence of each matching network on the PAE of any PA can be evaluated by the gain of the PA. The impact of each block on the PAE of the PA is inversely proportional to the gain of each stage that provides the overall gain. Since the effect of the TMNs (except for the output stages) on the power efficiency is minor, we can perform a reasonable trade-off between the insertion loss and other factors such as bandwidth or compactness of the matching networks. With this understanding, the



resistance matching issue in the inter-stage and the input stage presented in the *previous* sub-section can be alleviated.

*b) Design considerations of the output stage*

It is a natural choice to design the PA from the output stage to the input stage consecutively when considering the importance of the larger signal toward the output stage. There are trade-offs in choosing the active device size for the output stage. A large-sized transistor is preferable for high output power. However, two issues need to be considered regarding its output and input impedance matchings. The output impedance of a transistor can be modeled by a parasitic capacitor ( $C_{op}$ ) in parallel with an output resistor ( $R_{op}$ ), and this model applies to the large signal as well. When the output transformer (i.e., TF<sub>4</sub>) has the impedance transformation ratio of  $T_{im}$  and its primary inductance perfectly resonates out  $C_{op}$ , then  $R_{op}$  should be  $R_{opTF} = R_L * T_{im}$  ( $R_L$  is the load impedance) to attain the maximum efficiency  $\eta_{max}$ . However, the device size can be further increased to enhance the output power in a trade-off with degradation of the power efficiency. When the device size is increased by  $n$  times ( $n > 1$ ), the output resistor,  $R_{op}$ , roughly decreases by  $n$  times. Then, the new efficiency  $\eta$  can be calculated through the maximum efficiency  $\eta_{max}$  by the ratio  $r_e$  as

$$r_e = \frac{\eta}{\eta_{max}} = 1 - \left( \frac{n-1}{n+1} \right)^2 = \frac{4n}{(n+1)^2}. \quad (4.2)$$

The ratio of the new saturated output power  $P_{sat}$  to  $P_{sat0}$  at the maximum efficiency becomes:

$$r_p = \frac{P_{sat}}{P_{sat0}} = n \left( 1 - \left( \frac{n-1}{n+1} \right)^2 \right) = \frac{4n^2}{(n+1)^2}. \quad (4.3)$$

Figure 4.3 presents the ratio of efficiency decrease ( $r_e$ ) and power increase ( $r_p$ ) versus  $n$  which shows that  $r_p$  increases faster than  $r_e$  decreases, particularly in the small region of  $n$ . Thus, we can see a small amount of the efficiency degradation can be well traded off for relatively larger output power.



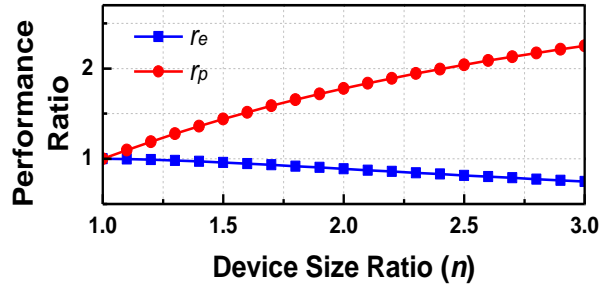


Figure 4.3. Power gain and efficiency compression ratios ( $r_e$  and  $r_p$ ) versus the increased ratio of the active device size ( $n$ ).

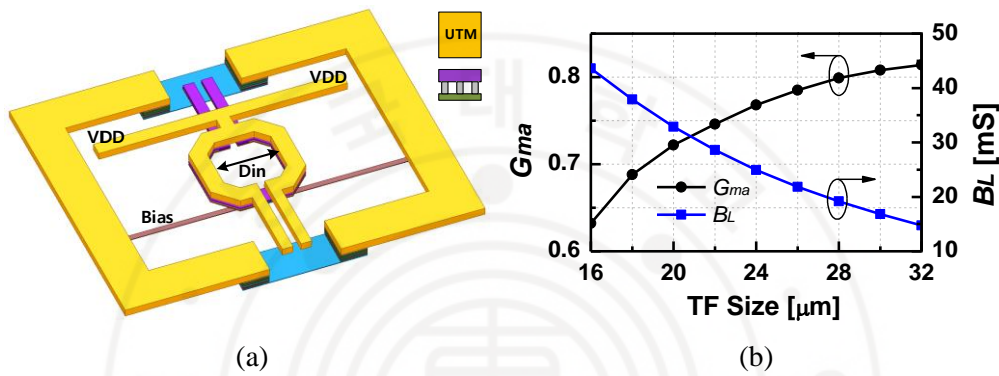


Figure 4.4. Implemented transformer structure in 65-nm CMOS (a) and the extracted optimal load susceptance ( $B_L$ ), and the maximum available gain ( $G_{ma}$ ) of transformers with different inner diameter sizes ( $D_{in}$ ) (b).

There is another aspect to be considered when choosing the output active device size which is related to its preceding transformer (i.e., TF<sub>3</sub>). A larger transistor size ( $M_3$ ) requires a smaller transformer (TF<sub>3</sub>) to resonate out its increased gate capacitance. However, the reduced magnetic coupling of the small size results in a high-loss transformer implementation. To investigate the effects of the reduced magnetic coupling, we simulated various transformers of different inner diameters ( $D_{in}$ ). The realized structure of the transformers is shown in Figure 4.4a. Herein, the on-chip transformer is constructed from three metal layers. The ultra-thick metal layer (UTM) forms the primary coil, aiming to carry the large drain quiescent current. Meanwhile, the two metal layers below the UTM are combined for the secondary coil. The inner diameter of the transformer is denoted by  $D_{in}$  and the width of the winding is  $W=6\ \mu\text{m}$ . The length of the two ports is fixed to be  $25\text{-}\mu\text{m}$  to keep a certain distance between the windings and the surrounding ground. Each winding of the transformer has a center tap for VDD and gate biasing. The extracted optimal load susceptance ( $B_{Lopt}$ ) and maximum available gain ( $G_{ma}$ ) of the transformers in different sizes

are presented in Figure 4.4b. We can observe that the transformer efficiency is degraded quickly as the transformer size decreases due to the reduced magnetic coupling. When we reduce the transformer diameter  $D_{in}$  from 32  $\mu\text{m}$  to 16  $\mu\text{m}$ ,  $G_{ma}$  drops by about 20%, and the extracted  $B_{Lopt}$  increases from 14.8 mS to 43.6 mS. This means the output transistor size supported by the 32  $\mu\text{m}$  transformer is expected to be nearly three times smaller than that of the 16  $\mu\text{m}$  transformer.

In this analysis, it was assumed that the maximum generated output power and the parasitics of the transistor are linearly proportional to its size. However, in practice, the efficiency of a large transistor can be noticeably degraded due to the long routing line with bottom metal layers in the device layout. We designed various transistors at different sizes using the ‘table structure’ with eight cells to investigate this effect as shown in Figure 4.5. The gate capacitance of the transistors was extracted to select the suitable preceding resonant transformer (i.e., TF<sub>3</sub>). Load-pull simulations were performed on the output transistors with their selected transformer-based input matching networks, and the simulation results are shown in Table 4.1.

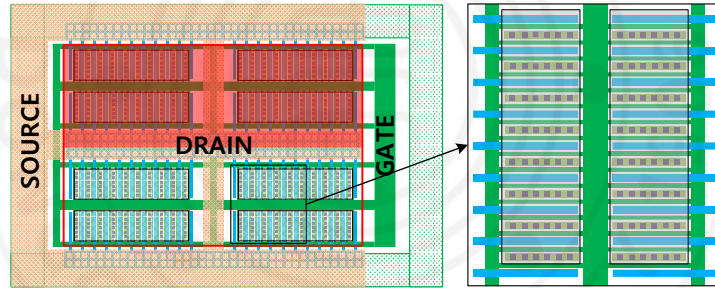


Figure 4.5. Simplified layout of a transistor using a table structure.

Table 4.1. Performance of the output transistor at different sizes.

Output transistor width ( $\mu\text{m}$ )	Suitable input transformer size ( $\mu\text{m}$ )	$P_{max}$ (mW)	PAE (%)	$R_{op}$ ( $\Omega$ )
80	~28	41.7	45.9	71.7
104	~25	50.9	45.4	61.5
128	~22	58.9	44.5	52.3
152	~20	65.3	43.3	45.0
176	~18	70.5	41.6	38.6
200	~17	73.1	39.1	34.2

It is noticed that the required impedance transformation ratio,  $T_{im}$ , of the output transformer (TF<sub>4</sub>) is roughly close to unity for the optimal power efficiency from Table 4.1. Thus, a 1:1 turns ratio is selected for TF<sub>4</sub>. The optimal size of M<sub>3</sub> for the output impedance

matching is expected to be around  $W = 128 \mu\text{m}$ . Based on the analysis, the width of  $M_3$  was slightly increased by  $W = 168 \mu\text{m}$  from the optimal size to achieve higher output power. With the selected output transistor,  $D_{in} = 18 \mu\text{m}$  was chosen for  $TF_3$ , which could resonate with the large output transistor  $M_3$  to achieve a good trade-off between the expected output power and efficiency. The output transformer ( $TF_4$ ) was designed as large as possible for a given transistor to improve the overall power efficiency. The output transformer was designed to be  $24 \mu\text{m}$  so that the susceptance of the single-ended terminal compensates for the parasitic capacitance of the RF pad at the output port. Through the proposed approach, the maximum possible size of the output transformer can be chosen for improved power efficiency. On the primary side of  $TF_4$ , an additional capacitor  $C_4 = 4 \text{ fF}$  is required to compensate for its primary coil inductance. A MOM capacitor with a tailored layout was used for the compact matching of the primary coil, and its capacitance was extracted using Calibre™.  $C_2$  and  $C_3$  were also implemented in the same way.

### c) Design of gain stages

The active device size of the first ( $M_1$ ) and the second ( $M_2$ ) driving stages were determined considering the optimal efficiency. The device size was reduced compared with that of the output MOSFET, but it must be large enough to drive their load (i.e., their next stage). In this 65-nm CMOS process, each amplifier stage had an estimated gain of around 7 to 8 dB after impedance matching, and a power gain compression of 3 to 4 dB was observed when the output power ( $P_{out}$ ) became saturated with a large input power level. Thus, it is roughly estimated that the driving stage should provide an output power of 3–4 dB less than that at the output stage to achieve the full drive. Assuming that the maximum output power is proportional to the device size, we can initially set the active device size of the driving stage to half of that of the output stage. Because the gate biasing voltages for  $M_1$  and  $M_2$  were set to 0.6 V for improved efficiency, the device size was set to slightly larger than the expected size.

To ensure the two driving stages can drive the output stage to its maximum saturated power and achieve a good  $OP1dB$  level, an iterative process was performed on the device sizes of  $M_1$  and  $M_2$  with the initial device sizes estimated. All other transformer-based matching networks were designed in the same procedure as for  $TF_4$  at the output stage. The final device sizes for  $M_1$  and  $M_2$  were 60 and 88  $\mu\text{m}$ , respectively. Notably, DC-current consumption by  $M_1$  is marginal compared with that by  $M_3$ . Hence, we could choose a larger

$M_1$  size than expected to provide a higher gain. The relatively large gate capacitances of  $M_3$ ,  $M_2$ , and  $M_1$  determine the size of  $TF_3$ ,  $TF_2$ , and  $TF_1$ , respectively, so that each gate capacitance resonates out the secondary inductances of the corresponding transformers. In this way, it was not necessary to add tuning capacitors for the gate of each transistor. However, on the primary side of  $TF_2$  and  $TF_3$ , additional capacitors  $C_2=30$  fF and  $C_3=45$  fF were added to the corresponding drains to ensure the matching. Specifically, in the case of  $TF_1$  with a single-ended-to-differential configuration, the center tap of the primary winding is connected to the ground to reduce the parasitic capacitance. Because of this connection, an extra capacitor  $C_1$  of 34 fF was needed to make it resonate with the primary inductance of  $TF_1$  along with the parasitic capacitance from the input RF pad. The gate bias lines for  $TF_1$ ,  $TF_2$ , and  $TF_3$  were connected in series with 5k- $\Omega$  resistors to avoid a potential common-mode oscillation caused by the parasitic inductances of the biasing lines. The W-band push-pull PA was fabricated in 65-nm CMOS process. The photograph of the fabricated chip is presented in Figure 4.6. The core size of the designed PA is only 0.05 mm<sup>2</sup> while the total area including RF pads is 0.435 mm<sup>2</sup>.

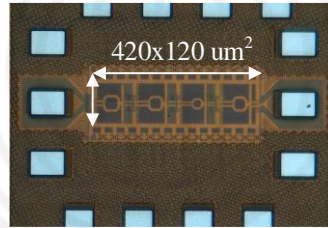


Figure 4.6. A Photograph of the fabricated 77-GHz PA in a 65-nm CMOS.

#### 4.2.2 Measurement results

In the measurement, the PA consumed a DC-current of 95 mA from a 1.3-V supply without input signals. The measurement setup for S-parameters and large-signal performances are illustrated in Figure 4.7. A vector network analyzer (VNA), Keysight N5224A (10 MHz to 43.5 GHz) combined with an extension module was used with an on-wafer probe station to measure the S-parameters of the PA. The on-wafer setup was calibrated using a calibration kit (CS-5). The measured S-parameters of the PA are presented in Figure 4.8 in comparison with the simulation results. It achieved a peak power gain of 22.6 dB at 77-GHz and a 3-dB bandwidth of 9 GHz (72.5–81.5 GHz), which corresponds well with the simulation results. The measured reverse isolation ( $-S_{12}$ ) is better than 45 dB.

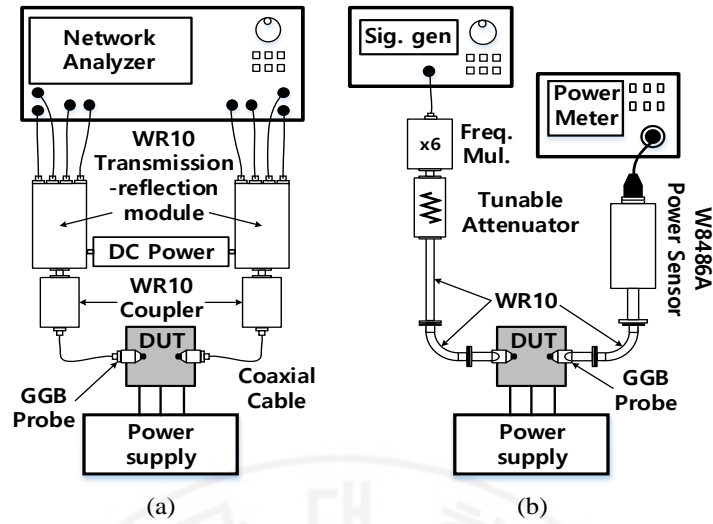


Figure. 4.7. Measurement setup for (a) S-parameters and (b) Large-signal performances.

In the large-signal measurement, a signal generator with a stand-alone frequency multiplier was used to generate W-band signals and a tunable attenuator was used to sweep the input power level. The insertion losses of the probe tips and the WR-10 waveguides were measured and calibrated from the raw data. The measurement results for the PA in terms of output power, output 1-dB gain compression point ( $OP1dB$ ), and power-added efficiency ( $PAE$ ) as a function of the frequency are presented in Figure 4.9. The measured output power, gain, and  $PAE$  at 77-GHz and 79-GHz are shown in Figure 4.10. The fabricated PA achieved a maximum  $P_{sat}$  of 16.4 dBm with a peak  $OP1dB$  of 13.6 dBm and a peak  $PAE$  of 20.3% recorded at 79 GHz. Over the band of interest (76-81 GHz), the measured saturate output power varies within 0.6-dB from its peak. The performances of the proposed PAs are summarized and compared with recently reported CMOS PAs at similar frequencies in Table 4.2. The implemented 77GHz PA in this work attained well-balanced small-signal and large-signal performances and, to the best of our knowledge, its achieved power density is among the highest score for a bulk CMOS PA in W-band.



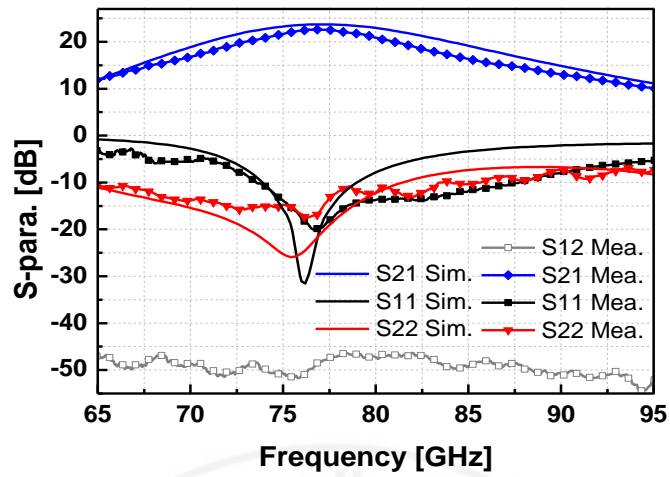


Figure 4.8. Simulated and measured S-parameters of the 77-GHz PA.

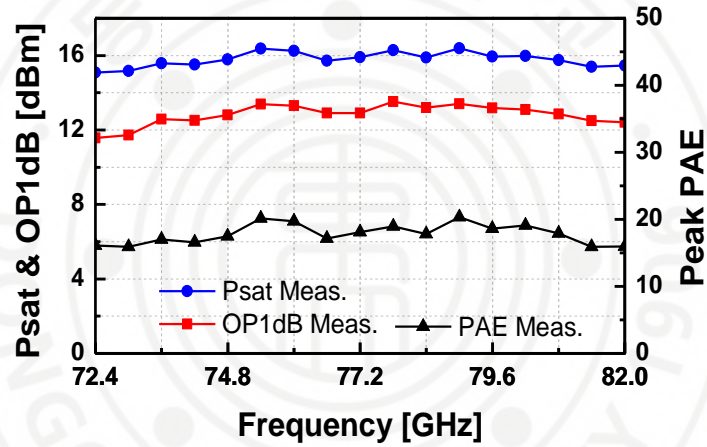


Figure 4.9. Measured saturated output power ( $P_{sat}$ ), output 1-dB gain compression point, and PAE versus frequency.

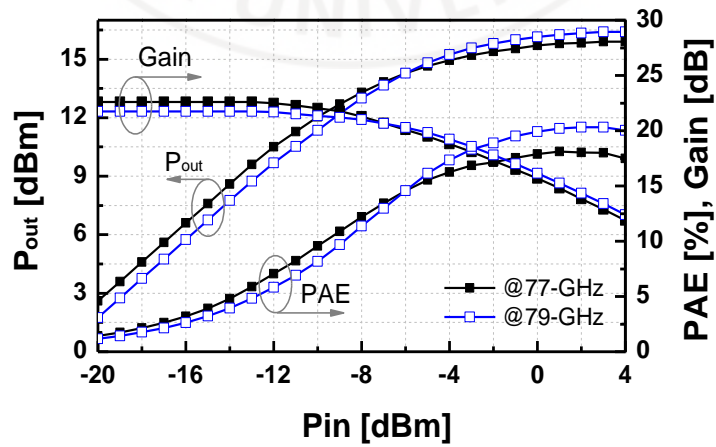


Figure 4.10. Measured output power ( $P_{out}$ ), gain, and PAE versus input power.



Table 4.2. Summary of state-of-art mm-wave CMOS PAs around 77 GHz

Ref.	CMOS Tech.	Com. way	Freq. (GHz)	$P_{sat}$ (dBm)	Gain (dB)	Peak PAE (%)	OP1dB (dBm)	Core Area (mm <sup>2</sup> )	DC-Diss. (mW)	$P_{sat}/Area$ (mW/mm <sup>2</sup> )
<b>This</b>	<b>65 nm</b>	1-way	<b>72.5-81.5@77</b>	<b>16.4</b>	<b>22.6</b>	<b>20.3</b>	<b>13.6</b>	<b>0.05</b>	<b>124</b>	<b>873</b>
[4.11]	65-nm	1-way	77	13.2	NA	17.6	NA	NA	0.17	-
[4.27]	65-nm	2-ways	84.0-88.8@87	11.9	18.6	9.0	9.6	0.23*	NA	67
[4.22]	65-nm	1-way	68-78@75	17.3	21.4	18.9	14.6	0.09*	284.7	597
[4.29]	65-nm	2-ways	74-82.5@77	15.8	26.4	15.9	11.5	0.14*	240	272
[4.31]	40-nm	4-ways	73	22.6	25.3	19.3	18.9	0.25*	NA	728
[4.24]	65-nm	1-way	76.8-83.8@81.6	16.3	28.3	14.1	13.6	0.121	234	353
[4.37]	65-nm	2-way	76-81	16.1	30	12.8	12.2	0.34	365	120
[4.38]	65-nm	8-way	74.3-86.2@77	15.4	24.4	10.4	12.1	0.42*	336	83
[4.13]	65-nm	1-way	73	14.29	26-31	22.37	12.03	0.033	120	813
[4.39]	40-nm	4-way	72	21	NA	13.6	19.2	0.19	NA	663
[4.40]	40-nm	4-way	70.3-85.5	20.9	18.1	22.3	17.8	0.19	375	648
[4.41]	28-nm	2-way	78	15.7	13.8	8.9	NA	NA	NA	-
[4.42]	22-nm SOI	1-way	76	17.8	17.8	17.3	13.3	0.02	260	3049
[4.12]	28-nm SOI	1-way	77	13.5	26.5	14.5	10	0.14	150	160

\* Estimated from the chip photo

### 4.3 Power amplifier design using power combiner beyond the SRF

#### 4.3.1 Operation of power combiner beyond the SRF

Because of the reciprocity of the on-chip passive elements, a passive PC can be used as a PS. Analyzing a PC can therefore be applied to its PS as well.

##### a) Equivalent Two-port Network of a Multiport PC/PS

Consider an  $n$ -way PC consisting of  $n$  input ports indexed from 1 to  $n$  and one output port, as illustrated in Figure 4.11(a). The current matrix  $[I]$  of the  $n+1$ -port network is calculated through its  $Y$ -parameter matrix  $-[Y]$  and the voltage matrix  $-[V]$ , as given by

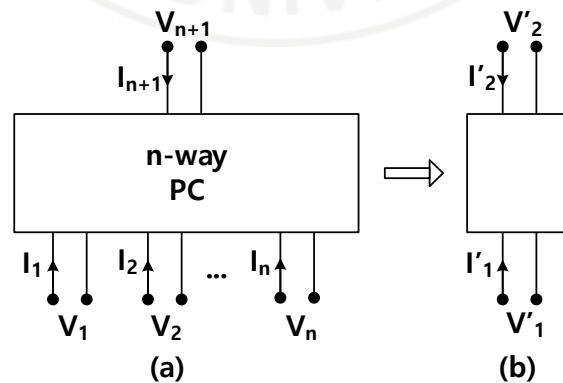


Figure 4.11. An  $n$ -way power combiner (a) and its equivalent two-port (b) when the voltages are identical at all the input ports.

$$\begin{bmatrix} I_1 \\ I_2 \\ \dots \\ I_{n+1} \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & \dots & y_{1,n+1} \\ y_{21} & y_{22} & \dots & y_{2,n+1} \\ \dots & \dots & \dots & \dots \\ y_{n+1,1} & y_{n+1,2} & \dots & y_{n+1,n+1} \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \\ \dots \\ V_{n+1} \end{bmatrix}. \quad (4.4)$$

As long as all of the voltages in the  $n$  input ports are the same (*i.e.*  $V=V_i$  ( $i = 1, \dots, n$ )), then (4.4) can be written as follows:

$$\begin{bmatrix} I_1' \\ I_2' \end{bmatrix} = \begin{bmatrix} y_{11}' & y_{12}' \\ y_{21}' & y_{22}' \end{bmatrix} \times \begin{bmatrix} V_1' \\ V_2' \end{bmatrix} \quad (4.5)$$

where  $I_1'$  is the sum of  $I_i$  ( $i=1, \dots, n$ ),  $I_2'=I_{n+1}$ ,  $V_1'=V$ ,  $V_2'=V_{n+1}$ . Figure 4.11(b) shows an equivalent two-port network formed by connecting all input ports with the same voltage. The Y-parameters of the two-port network is expressed by

$$\begin{aligned} y_{11}' &= \sum_{i=1}^n \sum_{j=1}^n y_{ij}; & y_{12}' &= \sum_{i=1}^n y_{i,n+1} \\ y_{21}' &= \sum_{i=1}^n y_{n+1,i}; & y_{22}' &= y_{n+1,n+1} \end{aligned} \quad (4.6)$$

The power losses in the  $n$ -way PC are calculated as

$$P_{loss} = \frac{1}{2} \sum_{i=1}^{n+1} V_i I_i^* = \frac{1}{2} \left( \sum_{i=1}^n V_i I_i^* + V_{n+1} I_{n+1}^* \right) = \frac{1}{2} (V_1' I_1'^* + V_2' I_2'^*), \quad (4.7)$$

where  $X^*$  denotes the complex conjugate of complex number  $X$ . Therefore, we have shown that calculating the loss of an  $n$ -way PC leads to the formulation of the loss in the equivalent two-port network (E2PN). Therefore, the maximum available gain ( $G_{ma}$ ) of the E2PN is the upper bound of the efficiency of the symmetric  $n$ -way PC. Because this value only depends on the network itself regardless of the outside environment, its absolute value (*i.e.*,  $|G_{ma}|$ ) is the *intrinsic loss* of the symmetric  $n$ -way PC. Moreover, the input admittance of the two-port network is the total input admittance of the  $n$ -way PC, which is given by

$$Y_{in}' = \frac{I_1'}{V_1'} = \frac{\sum_{i=1}^n I_i}{V_1'} = \sum_{i=1}^n \frac{I_i}{V_i} = \sum_{i=1}^n Y_{in-i} \quad (4.8)$$

If all the current values at the  $n$  inputs of the  $n$ -way PC are the same, then we obtain

$$Y'_{in} = nY_{in} \quad (4.9)$$

From this, the admittance seen from one port of the  $n$ -way PC is clearly defined when all of the input ports are electrically symmetric. A current PC constructed from the distributed elements such as a transmission line inherits their broadband-operation characteristic. Hence, the electrically symmetrical condition as mentioned above is applicable over a wide frequency range. In contrast, PCs established from lumped components such as transformers typically have their electrical characteristics limited to the SRF [4.43]. Beyond the SRF, the electrical symmetry is broken, thus the concepts of E2PN and its  $G_{ma}$  are inapplicable.

*b) Assessment of the SRFs of the Transformers and Voltage PCs via  $G_{ma}$*

A differential to a single-ended (D2SE) transformer as a balun is the special case of an  $n$ -way PC where  $n = 1$ , which is also considered to be a two-way PC with two single-ended inputs combined into one single-ended output. Figure 4.12(a) shows the realization of a 1:1 transformer in the 65-nm process using three metal layers. The on-chip transformer structure was built similar to that in other PA designs. The inner diameter of the transformer is denoted by  $D_{in}$  and the width of the winding was set at  $W = 6 \mu\text{m}$ . The length of the two ports was fixed at  $25 \mu\text{m}$  to keep a certain distance between the windings and the surrounding ground.

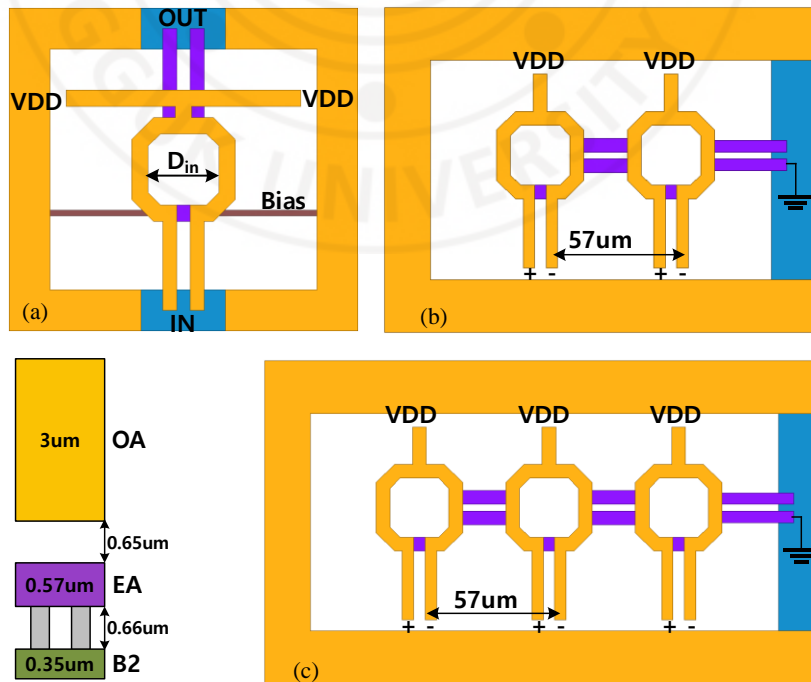


Figure 4.12. The implementation of (a) the transformer and PCs/PSs in the voltage domain, (b) a 2-way PC/PS, and (c) a 3-way PC/PS in the HFSS.

Similarly, the implementations of the 2- and the 3-way PCs in the voltage domain (PCV) using the 26  $\mu\text{m}$  transformer are shown in Figure 4.12(b) and (c), respectively. The distance between the two vicinity units was set to 57  $\mu\text{m}$  by considering the realized PA layout. Figure 4.13 shows the maximum available gain values of the D2SE 26- $\mu\text{m}$  transformer and the E2PNs of the PCVs. Two observations can be made when comparing these three plots of  $G_{ma}$ . First, the SRFs of the 3-way and 2-way PCVs are 50 and 62 GHz, respectively which are much smaller than the value for the D2SE transformer (118 GHz). Second, within the frequency range up to the first SRF, the  $G_{ma}$  peak values of the transformer, the 2-way PCV, and the 3-way PCV were gradually reduced. In detail, the peak  $G_{ma}$  values of the transformer, 2-way PCV, and 3-way PCV were -1.25 dB at 73 GHz, -1.5 dB at 39 GHz, and -1.7 dB at 31.5 GHz, respectively. Hence, we can conclude that the higher order of PCs suffers from a lower SRF and higher power loss than the others due to the extra conductor windings.

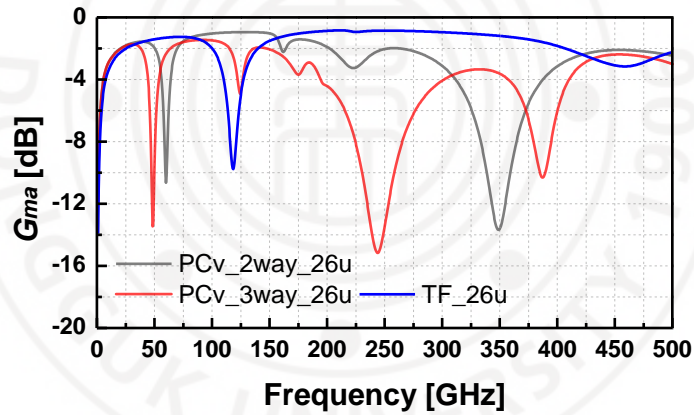


Figure 4.13.  $G_{ma}$  of the D2SE 26- $\mu\text{m}$  TF and the E2PNs of the two voltage PCs.

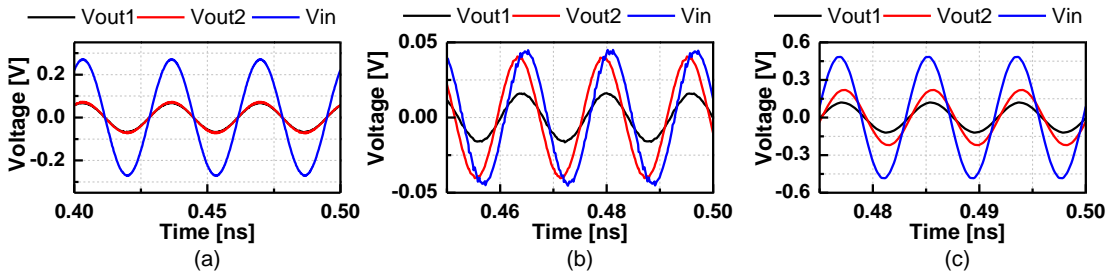


Figure 4.14. The simulated voltage waveforms of the two output ports ( $V_{out1}$  and  $V_{out2}$ ) and the input port ( $V_{in}$ ) of the 2-way PSV in Figure 4.11b when an input signal of 0-dBm is applied: (a)  $F_{in} = 30$  GHz, (b)  $F_{in} = 62$  GHz, and (c)  $F_{in} = 120$  GHz.

Notice that when the frequency approaches the SRF, the value of  $G_{ma}$  is inapplicable for the 2-way and 3-way PCs. To verify this, we excited the 2-way PCV as a PS in the voltage domain (denoted by PSV); i.e., port 3 was excited by using an input signal and the voltages at the two-unit ports were examined. Figure 4.14 shows the voltage waveforms at the two output ports ( $V_{out1}$  and  $V_{out2}$ ) and the input port ( $V_{in}$ ) when a different signal was applied at each frequency. In this experiment, the input port was connected to a 50- $\Omega$  signal source with an input power of 0 dBm, and the two output ports are attached to 100- $\Omega$  loads. It can be seen that when the input frequency  $F_{in} = 30$  GHz, the voltage waveforms of  $V_{out1}$  and  $V_{out2}$  were almost equal and in-phase with the input signal.  $V_{out1}$ ,  $V_{out2}$ , and  $V_{in}$  were different both in amplitude and phase when  $F_{in} = 62$  or 120 GHz. At the first SRF, the input impedance of the 2-way PSV became extremely small, resulting in a very small input voltage swing of merely 86 mV<sub>pp</sub> compared with those at 30 GHz (540 mV) and 120 GHz (960 mV).

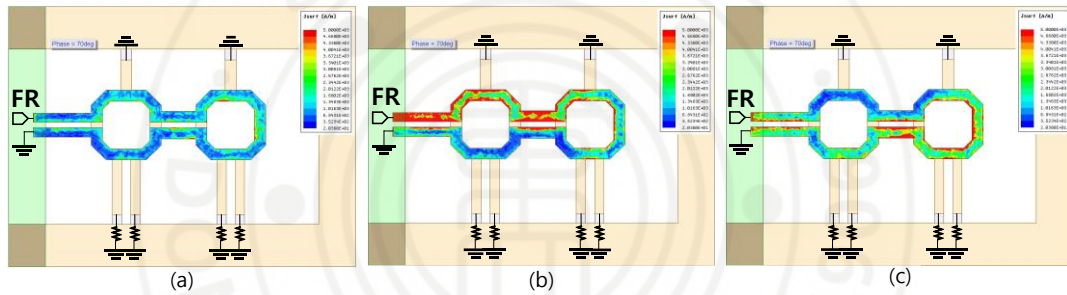


Figure 4.15. The simulated current distribution of the 2-way PSV shown in Figure 4.12b at different input-signal frequencies: (a)  $F_{in} = 30$  GHz, (b)  $F_{in} = 62$  GHz, and (c)  $F_{in} = 120$  GHz.

Under typical working conditions, the 2-way PSV shown in Figure 4.12(b) has one of the output ports connected to the ground and the other output port connected to a 50- $\Omega$  port. The input ports are connected to a 50- $\Omega$  load and the VDD ports are grounded on the AC-signal domain. Figure 4.15 shows a comparison of the current distribution of the 2-way PSV when working at 30 GHz (below the SRF), 62 GHz (at the SRF), and 120 GHz (over the SRF). It can be seen that the current was equally distributed on the whole routing coil when the PS works below the SRF. Meanwhile, the traveling wave with two cycles can be seen when the PS was working over the SRF. In particular, at the SRF, half of the PS structure formed a standing wave due to the resonance. Thus, the RF energy was mostly reflected in its source, resulting in a very low power transfer gain at this frequency. The whole

experiment further confirms the value of the SRF of PCVs/PSVs forecasted by using the concept of E2PN.

Even the maximum available gain of the E2PN of an  $n$ -way PC ( $n > 1$ ) is inapplicable when the frequency approaches its SRF, the graph of  $G_{ma}$  in Figure 4.13 can still be meaningfully used to evaluate the power loss of the transformer. After dropping down at the first SRF,  $G_{ma}$  recovered when the frequency further increased. Operating the transformer at the frequency band after the hump is called the second operational band. Likewise, the transformer might have higher SRFs, and the bands between them where the transformer has a small enough loss are the higher operational bands. The second operational band has a larger bandwidth than the first operational band, as can be seen in Figure 4.13. Interestingly, in the second operational mode, the peak  $G_{ma}$  of the transformer was  $-0.84$  dB at 214 GHz, which is better than the peak value in the first operational band. Theoretically, we expect higher operational bands at higher frequencies. However, in a real scenario, the higher resonance bands cannot be observed clearly because of the drastically increased loss of the transformer at such high frequencies due to the skin effect and substrate loss.

#### 4.3.2 Design of 85-GHz eight-way power amplifier

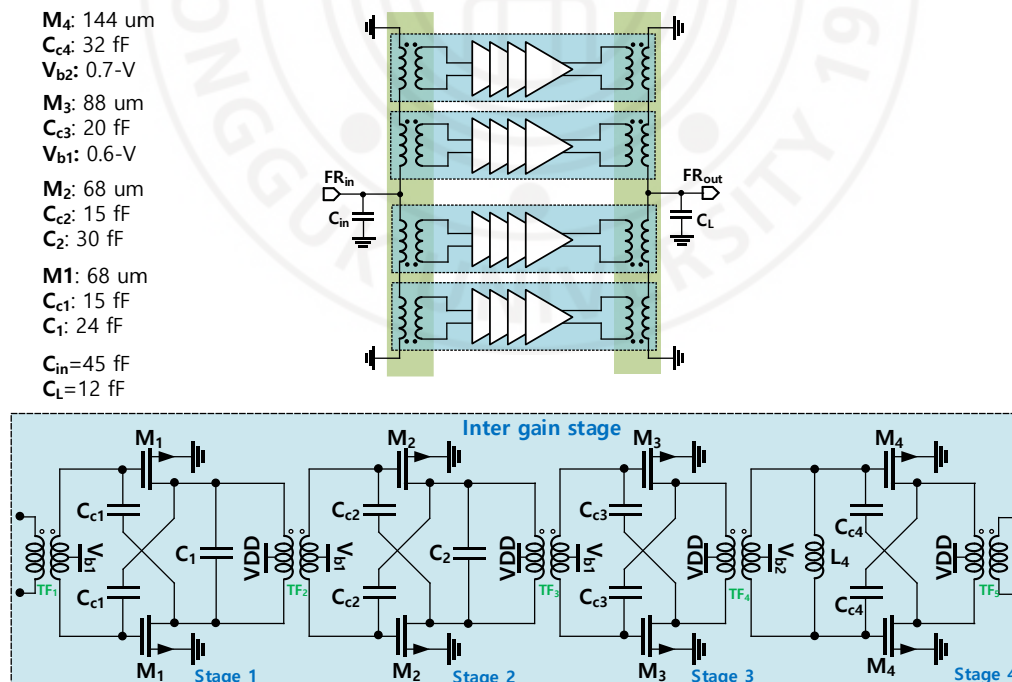


Figure 4.16. A schematic of a CMOS with the proposed W-band 8-way 4-stage PA using PC/PS in both the voltage and current domains.



A schematic of the proposed 8-way 4-stage PA is shown in Figure 4.16. The system consists of an input PS, a gain stage with four identical differential PA units, and an output PC. The inter-stage consists of four push-pull amplifiers using capacitive neutralization to enhance stability and impedance matching. In order to increase output power, VPC is used to provide an impedance matching mode that supports a larger active device size. Moreover, the 4-way PA is composed of two 2-way push-pull PAs combined in the voltage domain, which reduces the effective impedance twice, whereas each 4-way PA is combined in the current domain, which can raise the effective impedance seen from each 4-way PA by twice as much. Due to this, the effect of the two different power combining mechanisms on device size is compensated, so a proper device size can be chosen to improve the power efficiency and the current handling capability of passive embedding networks.

a) The Effect of Signal Imbalance on the PC's Performance

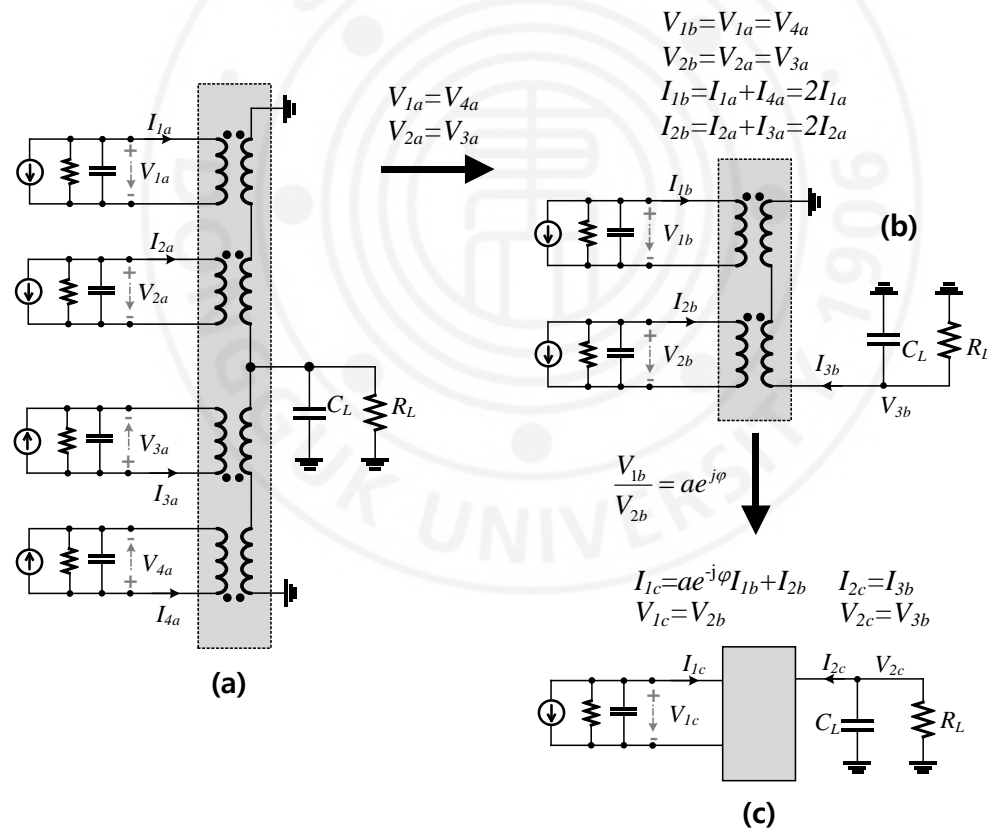


Figure 4.17. Equivalent circuits of the output PC.

A schematic for impedance matching at the output stage of the proposed PA is shown in Figure 4.17. The drain of the output stage MOS is modeled as a current source with

parasitic  $R$  and  $C$  in parallel, and a tuning capacitor  $C_L$  in parallel with the load  $R_L$  was used for impedance matching. Since the two current-combining branches in the 4-way output PC shown in Figure 4.17(a) are symmetrical, the two outside ports and the two inside ports can be connected in pairs to form an electrical equivalent 2-way PC (Figure 4.17(b)). The two input ports are labeled ports 1 and 2 and the output port is port 3. If the two signal sources generate the same voltages at their ports (*i.e.*,  $V_{1b}=V_{2b}$ ), then ports 1 and 2 can be connected to form an E2PN. In this case, the maximum efficiency of the PC,  $\eta_{PC\_max}$ , is bounded by the  $G_{ma}$  of the E2PN, which is simulated as -0.95 dB at 85 GHz. This efficiency is more promising compared to the value in the first SRF band. If  $V_{1b}$  is different from  $V_{2b}$  due to the loss difference, we can express the ratio between  $V_{1b}$  and  $V_{2b}$  as

$$\frac{V_{1b}}{V_{2b}} = ae^{j\varphi} \quad (4.10)$$

where  $a$  is the amplitude ratio and  $\varphi$  is the phase difference between  $V_{1b}$  and  $V_{2b}$ . In Figure 4.17, the efficiency of the PC is calculated by using

$$\eta = \frac{P_{out}}{P_{in}} = \frac{-\frac{1}{2} \operatorname{Re}(V_{3b} I_{3b}^*)}{\frac{1}{2} \operatorname{Re}(V_{1b} I_{1b}^*) + \frac{1}{2} \operatorname{Re}(V_{2b} I_{2b}^*)} \quad (4.11)$$

The numerator in (4.11) is the output power dissipated in the load and the denominator is the total power injected into the PC. Using (4.10), the input power  $P_{in}$  can be rewritten as

$$P_{in} = \frac{1}{2} \operatorname{Re} \left\{ V_{2b} \left( ae^{-j\varphi} I_{1b} + I_{2b} \right)^* \right\} \quad (4.12)$$

This is the equivalent power flowing into the input port with a port voltage of  $V_{1c} = V_{2b}$  and a port current of  $I_{1c} = ae^{j\varphi} I_{1b} + I_{2b}$ . The formula for the port voltages  $[V]$ , and current  $[I]$  using a Y-parameter matrix  $[Y]$  is given in (4.13) and rearranged in (4.14) as follows:

$$\begin{bmatrix} I_{1b} \\ I_{2b} \\ I_{3b} \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & y_{13} \\ y_{21} & y_{22} & y_{23} \\ y_{31} & y_{32} & y_{33} \end{bmatrix} \times \begin{bmatrix} V_{1b} \\ V_{2b} \\ V_{3b} \end{bmatrix} \quad (4.13)$$

$$\Rightarrow \begin{bmatrix} I_{1c} \\ I_{3b} \end{bmatrix} = \begin{bmatrix} y_{11c} & y_{12c} \\ y_{21c} & y_{22c} \end{bmatrix} \times \begin{bmatrix} V_{1c} \\ V_{3b} \end{bmatrix}, \quad (4.14)$$

where

$$\begin{aligned}
y_{11c} &= a^2 y_{11} + ae^{-j\phi} y_{12} + y_{21}ae^{j\phi} + y_{22} \\
y_{12c} &= ae^{-j\phi} y_{13} + y_{23} \\
y_{21c} &= ae^{j\phi} y_{31} + y_{32} \\
y_{22c} &= y_{33}
\end{aligned}
\tag{4.15}$$

Equation (4.14) represents the relationship between the currents and voltages in a two-port network in which one port has a voltage of  $V_{1c}$  and a current of  $I_{1c}$  while the other has a voltage of  $V_{2c} = V_{3b}$  and a current of  $I_{2c} = I_{3b}$ , as shown in Figure 4.17(c). This 2-port network is equivalent to the original 3-port PC network in terms of the power consumption by the input and output sides. Consequently, the maximum efficiency of the original PC is equal to the  $G_{ma}$  of the artificial 2-port network.

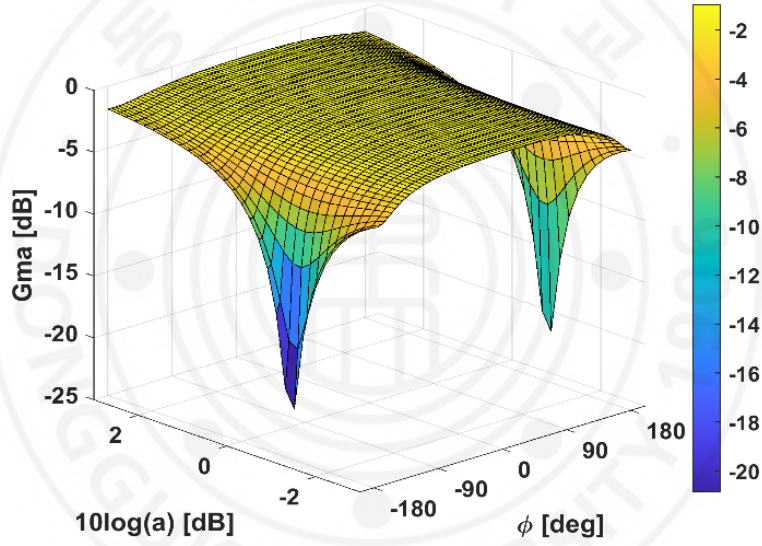


Figure 4.18. Simulated maximum efficiency at 85 GHz of the output PC versus the amplitude ratio ( $a$ ) and phase difference ( $\phi$ ) between  $V_{1b}$  and  $V_{2b}$ .

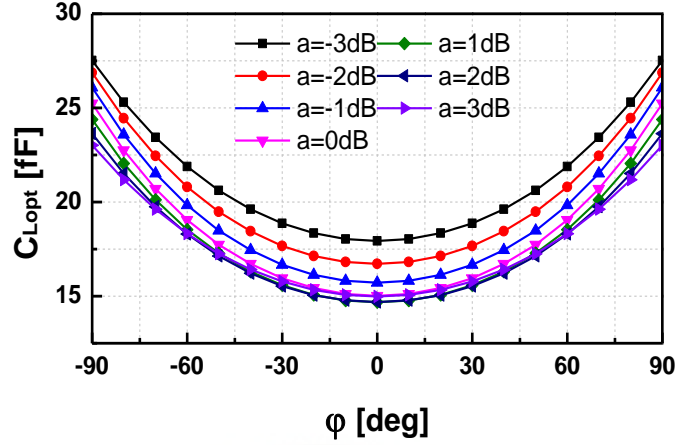


Figure 4.19. Calculated  $C_{Lopt}$  versus amplitude imbalance  $a$ , and phase imbalance  $\varphi$ .

The maximum efficiency of the output PCs as a function of the amplitude imbalance ratio ( $a$ ) and the phase difference ( $\varphi$ ) between  $V_{1b}$  and  $V_{2b}$  at 85 GHz is shown in Figure 4.18. In this extraction, EM simulations of the output PC under various values of  $a$  and  $\varphi$  were performed using HFSS, and the  $G_{ma}$  of the 2-port network was calculated from the extracted  $Y$ -parameters. The efficiency of the output PC drops drastically when the two voltages are in the reverse phase and their amplitudes are closed to -1.2 dB. Other than that, the maximum efficiency of the designed output PC was not much different from its peak value of -0.95 dB attained at  $a = 1.26$  and  $\varphi = 20^\circ$ , which can compensate for the effects of the path asymmetry of the designed PC structure. Ideally, the maximum efficiencies are still better than -1.5 dB within  $90^\circ$  of the absolute phase difference (*i.e.*,  $|\varphi| < 90^\circ$ ) and 3 dB of relative amplitude imbalance ratio (*i.e.*,  $|a| < 3$  dB). This result mitigates the requirement on the allowable amplitude and phase imbalance between the inside and outside signal paths.

The output PC and its equivalent networks presented in Figure 4.17(b) and (c) are passive networks that are naturally unconditionally stable. Their maximum power gain is attained under the condition of simultaneous conjugate impedance matching on both the input and output sides [4.44]. Based on the  $Z$ -parameters in [4.45], the optimal source ( $Z_{Sopt}$ ) and load ( $Z_{Lopt}$ ) and for a two-port network are respectively given by

$$\begin{aligned} Z_{Sopt} &= r_{11}(\theta_r + j\theta_x) - jx_{11} \\ Z_{Lopt} &= r_{22}(\theta_r + j\theta_x) - jx_{22} \end{aligned} \quad (4.16)$$

with parameters

$$\begin{aligned}
r_c &= \text{Re}\left\{\sqrt{z_{12}z_{21}}\right\}; \quad x_c = \text{Im}\left\{\sqrt{z_{12}z_{21}}\right\} \\
\theta_r &= \sqrt{\left(1 - \frac{r_c^2}{r_{11}r_{22}}\right)\left(1 + \frac{x_c^2}{r_{11}r_{22}}\right)} \\
\theta_x &= \frac{r_c x_c}{r_{11}r_{22}},
\end{aligned} \tag{4.17}$$

where  $z_{ij}=r_{ij}+jx_{ij}$  ( $i,j=1,2$ ) are matrix elements of the  $\mathbf{Z}$ -matrix.

The optimum tuning capacitor under a load can be derived as  $C_{Lopt}=\text{Im}\{Y_{Lopt}\}/\omega$ , where  $\omega$  is the angular frequency. For instance, if  $V_{1b}=V_{2b}$ , then the calculated  $Y_{Lopt} = 19.5+j8$  (mS) and  $Y_{Sopt} = 54.4+j81.5$  (mS), indicating that  $C_{Lopt} = 15$  fF and the total drain parasitic capacitance of the output transistors is 152.6 fF at 85 GHz. Figure 4.19 shows variation in the calculated  $C_{Lopt}$  according to the ratio of  $V_{1b}$  over  $V_{2b}$ . When  $|\varphi| < 90^\circ$  and  $|a| < 3$  dB, the value of  $C_{Lopt}$  varies from 15 to 27 fF, suggesting that the range of  $C_L$  is reasonable when it is co-optimized with other components in the whole PA circuit. The final value of the selected  $C_L$  is 12 fF by considering the additional parasitic capacitance of the pad, /which was simulated as  $\sim 7$  fF at 85 GHz. It is noticed that the bottom metal plate below the RF-pads was floated instead of being connected to the ground to achieve a small parasitic capacitance. On the input side, the input admittance of the 2-port network in Figure 4.17(c) can be calculated as

$$y_{in1c} = \frac{I_{1c}}{V_{1c}} = \frac{ae^{-j\varphi}I_{1b} + I_{2b}}{V_{2b}} = a^2 \frac{I_{1b}}{V_{1b}} + \frac{I_{2b}}{V_{2b}} = a^2 y_{in1b} + y_{in2b} \tag{4.18}$$

From (4.18), the optimal source admittance calculated for the two-port network in Figure 4.17(c) can be rewritten according to the optimal source admittances of the 3-port network in Figure 4.17(b) as follows:

$$y_{Sopt} = y_{in1c}^* = \left(a^2 y_{in1b} + y_{in2b}\right)^* = a^2 y_{Sopt\_1b} + y_{Sopt\_2b}, \tag{4.19}$$

where  $y_{Sopt1b}$  and  $y_{Sopt2b}$  are the optimal source admittances of port 1 and port 2 of the equivalent 3-port network in Figure 4.17(b), respectively. The effect of the source admittances of the inside and the outside signal paths on the optimized total source admittance differ by a factor of  $a^2$ . Along with the imbalance between the signal paths, this suggests that different MOS sizes should be chosen in each gain stage for different signal paths to achieve optimal power usage in the PA. However, utilizing different interstage amplifier designs makes the task of balancing their gain more complex, particularly in the

large-signal domain where different designs of the gain stages possess different characteristics of gain compression. In addition, design factors due to process variation create another issue when simulating the usage of identical designs for all the interstage gain amplifiers in the four signal paths. It is noticed that the input signals of the combiner generated by four stages of pseudo-differential amplifiers are expected to be highly differential. However, the electrical asymmetry of the primary coils of the combiner could distort these incoming differential signals, generating common-mode components at each input port. These common-mode components are naturally rejected by the combiner, causing further degradation of the overall PA's efficiency.

The device size of the output stage is initially selected based on the calculated optimal source admittance of the output PC under the assumption of  $V_{1b}=V_{2b}$ ; it can then be optimized in the large-signal domain to attain the largest output power. The final optimized width of the output transistor was 140  $\mu\text{m}$  when co-designed with the PC using a transformer with a diameter of 32  $\mu\text{m}$ . The output stage of the whole PA was simulated with Cadence Virtuoso, and the saturated output power of 20.5 dBm was recorded in the simulation.

A similar design procedure was applied for the input PS as well. However, different from the PC design, one deterministic signal source split into different signal paths generates differences in amplitude and phase between them. Moreover, the design criteria of the power efficiency for the PS are not as crucial as those for the PC due to the lower power level of the processed signal at the input. Although the power efficiency of the PC is not sensitive to an imbalance between each signal path (as mentioned above), the amplitude imbalance prevents the gain stage amplifiers from obtaining maximum simultaneous power capabilities, thereby degrading the overall power-added efficiency (PAE) of the PA. In this design, the input PS was designed with a small transformer with a diameter of 22  $\mu\text{m}$  to minimize the amplitude imbalance between the signal paths. Figure 4.20 shows the simulation results of the amplitude and phase imbalance between the outside port (port 1) and the inside port (port 2) of the input PS. As can be observed, the amplitude imbalance is within 1.4 dB and the phase imbalance is within  $4^\circ$  from 70 to 100 GHz. In the simulation, the whole PA achieved a peak PAE of around 11% at 85-GHz.



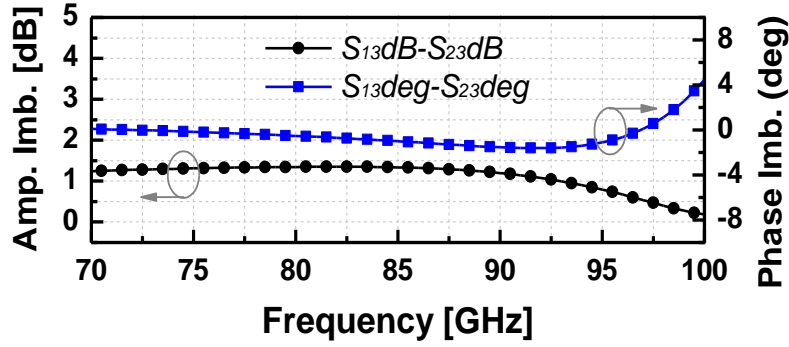


Figure 4.20. Simulated amplitude and phase imbalance between the inside port (port 1) and the outside port (port 2) to the input port (port 3) in the input PS.

*b) Design of the Inter-stage Gain Amplifier*

The inter-stage gain amplifier was constructed from four stages of compact push-pull amplifiers to support a high gain PA design to relax the requirement for the input power to drive the PA to the saturation region. The design sequence was performed from the output (stage 4) to the input (stage 1) based on the significance of the DC power consumption and the stage efficiency. The gate bias voltage for the power stage (stage 4) was chosen as 0.7 V to attain an enhanced output power, while the gate bias for the gain stages (from stage 1 to stage 3) was 0.6 V to achieve a good trade-off between the power gain and overall power efficiency. Transistor parameters, as well as DC current in each stage, are given in Table 4.3.

Table 4.3. Transistor parameters of the 8-way PA

Parameters	M <sub>1</sub>	M <sub>2</sub>	M <sub>3</sub>	M <sub>4</sub>	Units
Length ( <i>l</i> )	65	65	65	65	[nm]
Width ( <i>w</i> )	68	68	88	140	[ $\mu$ m]
Current ( <i>I<sub>DS</sub></i> )	9	9	12	30	[mA]

Table 4.4. Extracted parameters of transformers and inductor of the 8-way PA

TF	Inductance (pH)		<i>k</i>	<i>Q</i> -factor		<i>IL</i> (dB)
	Primary	Secondary		Primary	Secondary	
TF <sub>2</sub>	53	55	0.56	14.5	11.1	4.1
TF <sub>3</sub>	43	44.6	0.54	13.3	10.3	3.9
TF <sub>4</sub>	53	55	0.56	14.5	11.1	3.3
L <sub>4</sub>	70.1			9.2		

The transistors' sizing and their impedance matching with the transformer's networks were designed with a similar concept that was applied to previously presented PAs. Notably, the gate parasitic of the output stage was relatively large and thus, required a corresponding

small inductance to resonate. Hence, an additional shunt inductor was employed on the secondary side of the  $TF_4$  to resonate with the large gate parasitic to support a large-sized  $TF_4$  with a reasonable mutual coupling factor  $k$ . However, the low-quality factor of the small effective inductance realized in a compact area can cause efficiency degradation. The extracted parameters of the employed transformers are given in Table 4.4 along with the simulated insertion loss of the corresponding matching network. The active device was gradually tapered from the output to the input stage to optimize the power efficiency while still achieving the target of high gain performance. The final designed parameters of the circuit components of the gain stage amplifier are shown in Figure 4.16.

Owing to the compactness of the transformer-based push-pull amplifiers, we could alleviate the area occupancy of the whole PA with eight signal pathways connected in parallel. For each push-pull amplifier in the gain stage, the gate bias lines were connected in series with  $5k\text{-}\Omega$  resistors to avoid potential common-mode oscillation caused by the parasitic inductance of the biasing lines [4.46]. The stable operation of the PA was carefully verified because of potential inter-couplings between the signal pathways in such a dense space. In the small-signal domain, the stability factor ( $K\text{-}1$ ) of the whole PA was checked to verify the unconditionally stable condition. Moreover, a step function was applied to the supply voltage to excite any unrevealed potential instability trapped by the large signal excitation in the transient simulation.

#### 4.3.3 Measurement results

The proposed PA was fabricated in 65-nm CMOS process. The PA was implemented in an area of  $0.72\text{ mm}^2$  with a full pad size and only  $0.172\text{ mm}^2$  for the core PA. A microphotograph of the fabricated 85-GHz PA is presented in Figure 4.21. A vector network analyzer (VNA), Keysight N5224A (10 MHz to 43.5 GHz), combined with a W-band extension module (75–110 GHz) was used with an on-wafer probe-station to measure the S-parameters of the 85-GHz PA. The on-wafer setup was calibrated using a CS-5 calibration kit. The measured PA drew a DC-current of 485 mA from a 1.2-V supply.

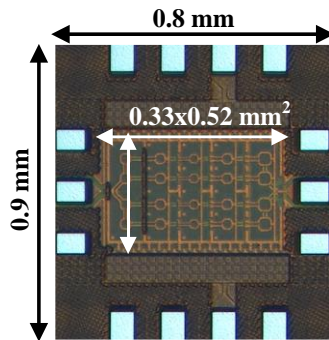


Figure 4.21. A photograph of the fabricated 8-way PA in 65-nm CMOS.

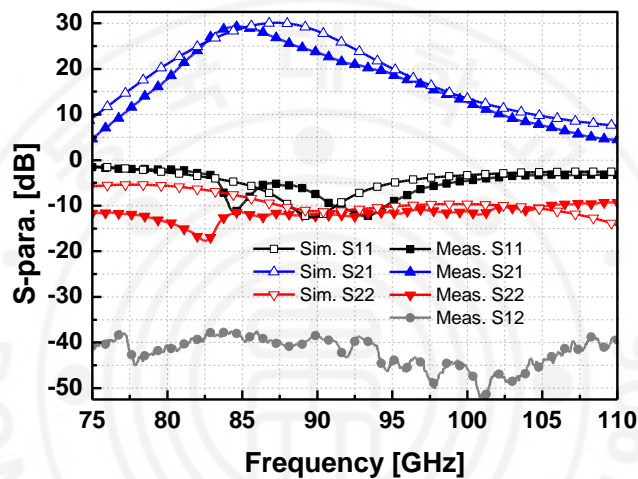


Figure 4.22. S-parameters of the 8-way PA on simulation and measurement.

The simulated and the measured S-parameter values of the PA are presented in Figure 4.22. The measured peak power gain ( $S_{21}$ ) was 29.3 dB at 84 GHz, and the measured 3-dB bandwidth was from 82.7–86.7 GHz. For large-signal measurements, a signal generator (Agilent 83623B) with a stand-alone frequency multiplier was used to generate E-band signals and a tunable attenuator was used to sweep the input power level. The insertion losses of the probe-tips and the WR-10 waveguides were measured and calibrated from the raw data.

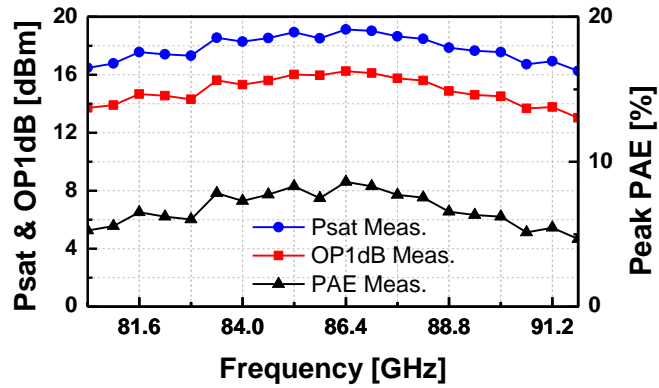


Figure 4.23. The measured  $P_{sat}$ , OP1dB, and PAE of the 8-way PA.

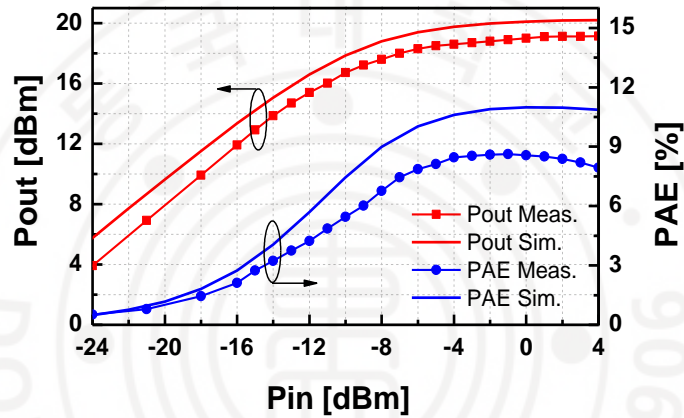


Figure 4.24. Simulated and measured output power ( $P_{out}$ ) and PAE of the 8-way PA according to input power ( $P_{in}$ ) at 86.4 GHz.

Table 4.5. Summary of State-Of-The-Art CMOS PAs around W-Band

Ref.	CMOS Tech.	Topology	Frequency (GHz)	VDD (V)	$P_{sat}$ (dBm)	Gain (dB)	Peak PAE (%)	OP1dB (dBm)	Core Area (mm <sup>2</sup> )	DC-Diss. (mW)	FOM <sub>i</sub>
<b>This</b>	<b>65nm</b>	<b>8-way PCV<sub>4</sub>I<sub>2</sub></b>	<b>82.7–86.7@84</b>	<b>1.2</b>	<b>19.1</b>	<b>29.3</b>	<b>8.6</b>	<b>16.2</b>	<b>0.172</b> <b>0.72*</b>	<b>582</b>	<b>41981</b>
[4.26]	65nm	4-way PCV <sub>2</sub> I <sub>2</sub>	100–117@109	1.2	15.2	20.3	10.3	12.5	0.103	NA	4342
[4.27]	65nm	4-way PCV <sub>2</sub> I <sub>2</sub>	84.0–88.8@87	1	11.9	18.6	9.0	9.6	0.37*	NA	764
[4.19]	90nm	4-way PCI <sub>4</sub>	86–98@94	2.4	16.8	20	16.4	15	0.69*	280	6936
[4.28]	65nm	4-way PCV <sub>2</sub> I <sub>2</sub>	77	2	15.8	20.9	15.2	13	0.21	246	4215
[4.20]	90nm	2-way PCI <sub>2</sub>	69–81@76	2.4	12.8	21.5	9.9	9.5	0.36*	182.4	1539
[4.22]	65nm	2-way PCV <sub>2</sub>	68–78@75	1.3	17.3	21.4	18.9	14.6	0.09	284.7	7881
[4.23]	40nm	2-way PCV <sub>2</sub>	92.5–117@110	1.8	12.2	25.5	8.5	10.3	0.076	NA	6056
[4.29]	65nm	4-way HCV <sub>2</sub>	74–82.5@77	1.2	15.8	26.4	15.9	11.5	0.14	240	15645
[4.30]	40nm	8-way PCV <sub>4</sub> I <sub>2</sub>	70.3–85.5@80	0.9	20.9	18.1	22.3	17.8	0.19	375	11337

[4.31]	40nm	8-way PCV <sub>1</sub> I <sub>2</sub>	73	1.8	22.6	25.3	19.3	18.9	0.25	NA	63417
[4.24]	65nm	2-way PCV <sub>2</sub>	76.8– 83.8@81.6	1.2	16.3	28.3	14.1	13.6	0.121	234	26461
[4.15]	45nm SOI	3-stack	91	3.4	19.2	12.4	14	NA	0.228	379	1676
[4.25]	28nm SOI	2-way PCV <sub>2</sub>	77	1	13.5	26.5	14.5	10	0.14	150	8597
[4.18]	45nm SOI	6-stack	85–90@86	6.8	19	36	8.9	NA	NA	NA	103.2

$$FOM_1 = P_{sat} \times Gain \times PAE \times f^2$$

\* PA full area including pads.

NA, not available; HC, hybrid coupler.

PCV<sub>n1</sub>I<sub>n2</sub>: power combining where  $n_1$  and  $n_2$  denote the number of combining ways in voltage and current domains, respectively.

Figure 4.23 demonstrates the saturated output power ( $P_{sat}$ ), output 1-dB gain compression point (OP1dB), and the peak PAE of the PA versus frequency on measurement. The implemented PA achieved a maximum  $P_{sat}$  of 19.1 dBm with a peak PAE of 8.6% and an OP1dB of 16.2 dBm at 86.4 GHz. Figure 4.24 shows the simulated and measured output power as well as PAE of the PA versus applied input power at 86.4 GHz. The performance of the proposed PA is compared with recently reported state-of-the-art CMOS PAs at similar frequencies in Table 4.5. The implemented PA in this work achieved one of the highest figure-of-merit (FOM) in both FOM<sub>1</sub> and FOM<sub>2</sub>. It is noted that the measured PAE is smaller than that in the compared PAs since the designed PA has four stages to achieve a high gain application. Increased loss from the small inductors used in driving the output transistors is another reason for the PAE degradation in trade-off with the enhanced output power. The proposed PA achieved the core size of 0.172 mm<sup>2</sup> with the demonstration of PCs /PSs which can operate beyond their SRFs with a promising efficiency performance at the E-band regime. The proposed method of using the E2PN in characterizing the passive PCs/PSs can be extended to any multiport network whose port voltages are predetermined.

#### 4.4 Push-pull power amplifier design using inductive feedback

##### 4.4.1 Power amplifier design

The schematic of the proposed four-stage push-push PA is shown in Figure 4.25. Each stage was designed sequentially, starting with the output (4th) stage and ending with the input (1st). There is a feedback inductor in each stage that connects the drain to the gate of the NMOS. Separating the DC-bias voltage of the two terminals was achieved with an AC-coupling capacitor. Each of the push-pull stages was examined through the stability factor ( $K-\Delta$ ) and maximum gain ( $G_{ma}$ ) with the feedback network in HFSS. This improved PAE can be attributed to the enhanced gain at the output stage. In Figure 2, the maximum stable

gain  $G_{ms}$ , maximum available gain  $G_{ma}$ , and stability factor  $K$  are plotted against frequency for various feedback inductors in the active device. To ensure  $\Delta$  is less than unity, its absolute value was also examined. Without the feedback network, the active device would be unstable. The feedback network produces stability with  $K>1$  for the device when used with an inductor ranging from 70 pH to 115 pH with  $Q=17$ . The feedback inductor at  $L=85$  pH increases the gain of the active device by around 3 dB and makes it less sensitive to variations in parasitics at 82 GHz.

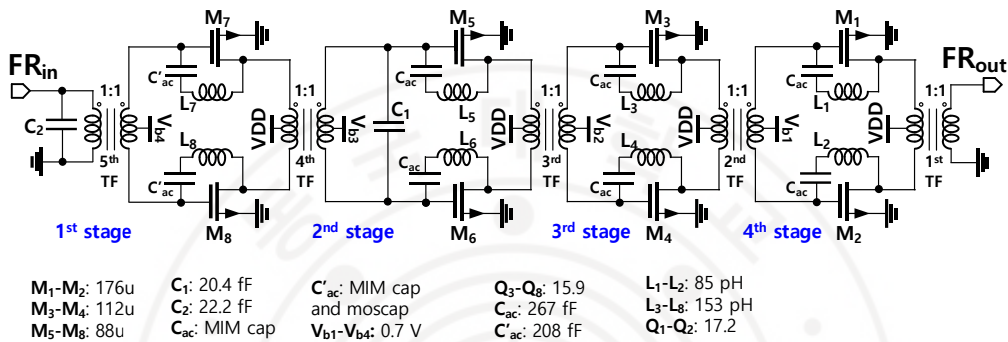


Figure 4.25. Schematic of the inductive feedback push-pull PA.

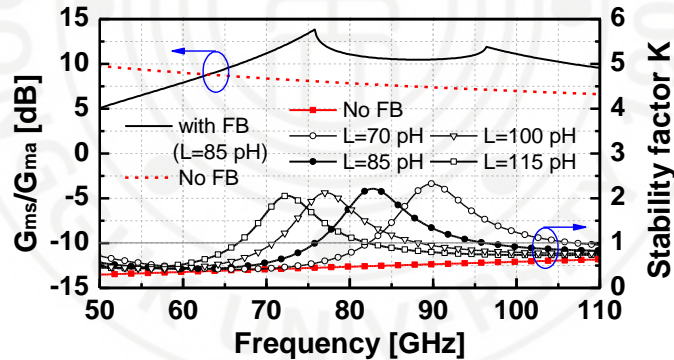


Figure 4.26.  $G_{ms}/G_{ma}$  and stability factor  $K$  against frequency in several values of feedback inductances.

Inter-stage impedance matching utilizing a transformer was carried out at 82 GHz to maximize the transducer power gain. The impedance matching method presented in chapter 1 was applied here to optimize the efficiency of the PA. By choosing the proper size of the secondary coil inductor of the output TF, the parasitic capacitance of the RF pad at the output stage was used as the shunt capacitance to resonate with the output TF. The output matching does not require an additional capacitor in parallel with the load. It is imperative to maximize the transistor size of the output stage to support high output power. To resonate with a large



gate capacitance with a small magnetic coupling factor, a large transistor requires a small TF, which may degrade the efficiency of transformation conversion.

Therefore, an optimal trade-off between the NMOS device size and TF insertion loss should be struck. In this design, an NMOS of  $W=176\ \mu\text{m}$  was chosen to support a reasonable efficiency TF for the output stage. From the output (4<sup>th</sup>) stage to the 2<sup>nd</sup> stage, the device size of each stage was gradually reduced to improve PAE. Unilaterization requires a bigger feedback inductance for a smaller transistor. In the third and second stages, transistor sizes are 112 and 88  $\mu\text{m}$ , respectively. For a compact PA design, the input (1st) stage has the same device size as the feedback inductor of the 2nd stage. For the de-Qing of the feedback network, the first stage of the design employed a MOS capacitor in parallel with the metal-insulator-metal (MIM) capacitor to facilitate impedance matching with the 50- $\Omega$  input source. The 1st stage output transformer was provided with a capacitive load by using an additional capacitor at the input ( $C_1$ ).

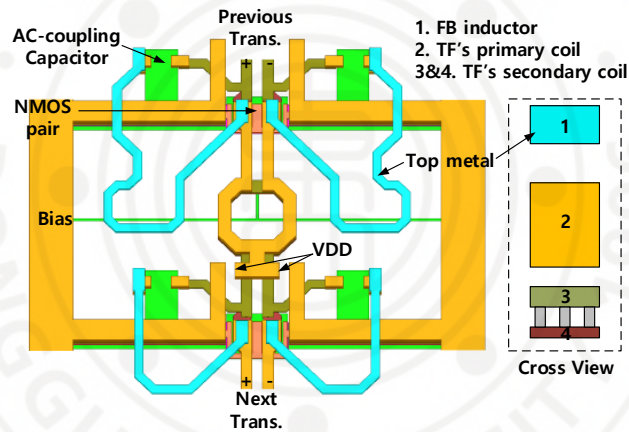


Figure 4.27. The physical layout of the feedback inductor for a push-pull PA.

Figure 4.27 shows the layout of the feedback inductors in the first and second stages. Inductors were implemented using top metal, while the transformer's primary coils were made of ultra-thick metal (UTM) to handle the drain current. The secondary coil of the TF was constructed from a stack of Metal 3 ( $M_3$ ) and Metal 4. We connected the gate biasing line in series with a 5-k $\Omega$  resistor to increase stability by suppressing the potential common-mode oscillations. The PA core occupies only 0.121 mm<sup>2</sup>. An image of the 82-GHz PA is shown in Figure 4.28.

#### 4.4.2 Measurement results

The PA has drawn a dc-current of 195 mA from a 1.2-V supply on measurement. The simulated and the measured S-parameters of the PA are shown in Figure 4.29. The peak power gain ( $S_{21}$ ) was measured to be 28.3 dB at 81.4 GHz, and the 3-dB bandwidth was around 7 GHz (76.8–83.8 GHz). These results corresponded well with the simulation values. Figure 4.30 presents the saturated output power ( $P_{sat}$ ), output 1-dB gain compression point (OP1dB), and the peak PAE of the measured PA. The fabricated PA achieves a maximum  $P_{sat}$  of 16.3-dBm; a peak PAE of 14.1% and an OP1dB of 13.6-dBm at 81.6 GHz. In the 3-dB gain measured bandwidth, the minimum  $P_{sat}$  dropped by 0.68 dB, and the OP1dB varied by 0.7-dB. The measured peak PAE fluctuated within 85-% of its highest value. Figure 4.31 shows the output power ( $P_{out}$ ) and PAE vs. input power ( $P_{in}$ ) at 81.6 GHz on simulation and measurement. The performances merits of the designed PA are summarized in Table 4.6 in comparison with other recent CMOS PAs at similar frequencies. The proposed push-pull PA using inductive feedback demonstrated an outstanding figure-of-merit among the recent W-band CMOS PAs to date.

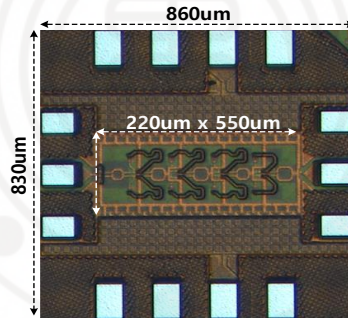


Figure 4.28. Photograph of the fabricated inductive-feedback push-pull PA.

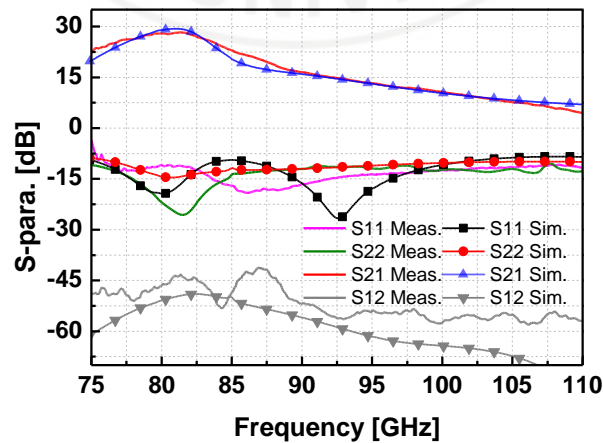


Figure 4.29. Simulated and measured S-parameters of the PA.

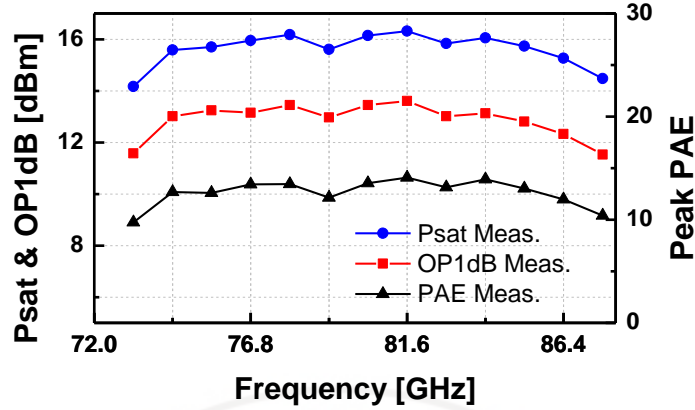


Figure 4.30. The saturated output power ( $P_{sat}$ ), output 1-dB gain compression point (OP1dB), and power-added efficiency (PAE) of the measured PA.

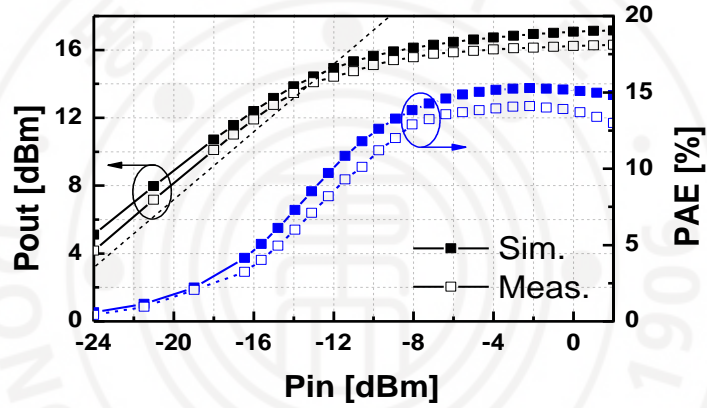


Figure 4.31. The measured and simulated output power ( $P_{out}$ ) and PAE versus input power ( $P_{in}$ ).

Table 4.6. Summary of the proposed PA with recent CMOS PAs in the W-band

Ref.	Tech. (CMOS)	Topology	Freq. (GHz)	$P_{sat}$ (dBm)	Gain (dB)	Peak PAE (%)	OP1dB (dBm)	Area (mm <sup>2</sup> )	DC-Diss. [mW]	FOM
[4.26]	65-nm	4-way com.	100-117@109	15.2	20.3	10.3	12.5	0.34	NA	86.4
[4.47]	65-nm	16-way com.	77-103@90	18.3	12.5	9.5	17.5	0.82	NA	79.7
[4.27]	65-nm	4-way com.	84.0-88.8@87	11.9	18.6	9.0	9.6	0.37	NA	78.8
[4.19]	90-nm	4-way com.	86-98@94	16.8	20	16.4	15	0.69	280	88.4
[4.28]	65-nm	4-way com.	77	15.8	20.9	15.2	13	0.21*	246	86.2
[4.20]	90-nm	2-way com.	69-81@76	12.8	21.5	9.9	9.5	0.36	182.4	81.9
[4.30]	40-nm	4-way com.	70.3-85.5@80	20.9	18.1	22.3	17.8	0.19*	375	90.5
[4.22]	65-nm	2-way com.	68-78@75	17.3	21.4	18.9	14.6	0.09*	284.7	89.0

[4.15]	45-nm SOI	3-stack	91	19.2	12.4	14	NA	0.228*	379	82.2
[4.14]	65-nm	2-way com.	57.2-66.9@~62	14.35	20.9	21.1	11.68	0.088*	126	84.3
<b>This</b>	<b>65-nm</b>	<b>2-way com.</b>	<b>76.8-83.8@81.6</b>	<b>16.3</b>	<b>28.3</b>	<b>14.1</b>	<b>13.6</b>	<b>0.72 (0.121*)</b>	<b>234</b>	<b>94.3</b>

\* The core only

$$FOM = P_{sat} \text{ (dBm)} + Gain \text{ (dB)} + 10 \log(PAE[\%] \times f^2 \text{ [GHz]})$$

## 4.5 Reference

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## V. Signal Generation in E-band

### 5.1 Introduction

High-quality local oscillators (LOs) are essential building blocks in advanced transceivers. LO architectures can be classified into fundamental oscillations and multiplications in combination with a low-frequency signal source. Traditionally, a conventional LC tank was used to generate signal oscillations in the direct generation structure. Due to the low-quality factor (Q) of the LC tank and the low capacitance ratio of the tunable components, this design approach suffers from poor phase noise (PN) and a narrow tuning range [5.1-5.3]. With oscillators designed at lower frequencies, tuning range and PN could be significantly improved. Thus, frequency multipliers (FMs) are increasingly used in millimeter-wave LOs. Moreover, the LO generation based on the use of on-chip FMs with an external low-frequency signal source is preferable for quick tests due to their wide tuning range and good PN performance of widely accessible outside signals [5.4].

Doublers and triplers are two commonly employed frequency multipliers (FM) that construct a designated multiplication factor (M). The triplers provide a larger multiplication factor, while it typically requires the active device to be biased at a considerable quiescent drain (or collector) current [5.5], [5.6]. Typically, the efficiency of the triplers significantly depends on the process variations since it depends on the non-linearity of the active device at a large bias voltage (around the triode region). By contrast, a push-push doubler works based on the superposition of two positive circles of the two input terminals, which naturally cancel out the odd harmonics at the single-ended output. Theoretically, the optimal bias point for the active device is at the threshold (knee) voltage. With this bias condition, the push-push doubler (PPD) can provide a steady performance over different technology nodes and achieve relatively high conversion efficiency with a low DC power consumption.

A common approach to implement a high order FM is to cascade multiple PPD. Since the output of PPD is inherently single-ended, this approach requires an output balun to drive the differential input of the next PPD stage. Unfortunately, the output signal of the realized balun with a winding transformer becomes naturally imbalanced because of the layout asymmetry. To avoid the use of the imbalanced balun with PPD, one can realize a doubler using Gilbert-cell (GC) for a differential output. However, the original GC doubler is strongly contaminated by the fundamental signal at its output since it is operating based on the self-mixing principle. By stacking two doubles and applying a tail resistor, a quadrupler

was introduced in [5.7], which could achieve approximately 30 dBc of HRR. However, this structure requires a high supply voltage to support the stacking of the four active devices. In [5.8], a differential-to-differential (D2D) doubler structure was implemented with a pair of PPD fed by two differential I/Q inputs. However, it necessitates a precise I/Q signal generation.

Some techniques to eliminate the output imbalance of the balun have been inherently applied in previous works. One of the typical methods to mitigate this imbalance is to put a filter next to the balun to suppress the unwanted harmonics. However, a high-order filter requires more area overhead in placing a bunch of LC passive components. It is noticed that a driving amplifier can also work as a bandpass filter (BPF) to reject the unwanted harmonics further. The second technique is to connect the center tap of the secondary side of the TF-based balun to the ground to form an electrical symmetry at the output [5.4]. However, common-mode oscillations due to the common inductor connected to the ground through the center tap of the balun can be excited, which may seriously disturb the proper operation of FM. This common-mode oscillation issue is more serious in CMOS due to the high impedance of the gate [5.9]. Another method to mitigate the imbalance issue is to use Marchand balun to attain quite low imbalance levels at the output at the cost of notably large area occupancy. Thus, it is particularly applicable at high frequency [5.10].

In this chapter, we present a novel circuit structure to mitigate the electrical imbalance at the transformers' output by using different capacitors connected to the two terminals. As demonstrated, this proposed method could significantly improve the harmonic rejection of a single PPD. Moreover, it also requires negligible area compared to a normal balun layout. By applying this technique, we designed a high-performance eight-time FM ( $\times 8$  FM) with three PPD stages which are followed by a driving amplifier (DA) implemented from push-pull amplifiers after each PPD. As a result, the designed FM could improve HHR by around 10-dB compared to conventional designs.

## **5.2 Design of an eight-time E-band frequency multiplier**

### *5.2.1 Transformer-based balun design using balancing capacitors*

#### *a) Effect of input imbalance on PPD output*

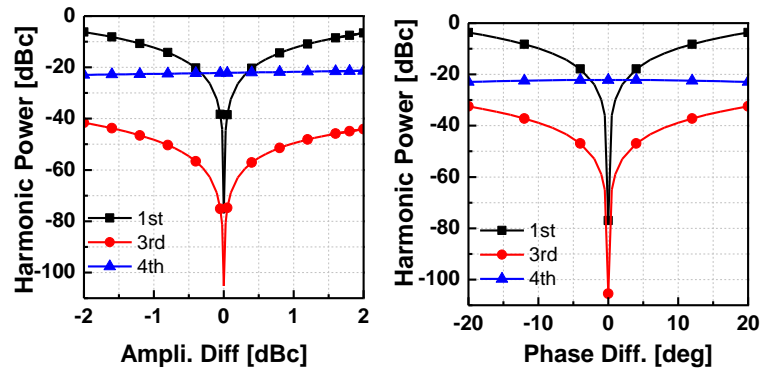


Figure 5.1. Effect of the unbalanced input on the harmonic rejection performance.

Based on the principle of superposition of two positive signal cycles, the PPD requires a highly balanced signal that has the same amplitude with an inverted phase at its differential input terminals to suppress all the odd harmonics at the output. Figure 5.1 shows the power levels of several harmonics around the main tone of a doubler versus the amplitude and phase imbalance. It is shown that the 1<sup>st</sup> and the 3<sup>rd</sup> harmonic power levels change quickly near the ideal condition where the odd harmonics can be perfectly eliminated at the common mode output of the doubler. Thus, a small amount of improvement in the phase and amplitude balancing would significantly enhance the HHR of the PPD. The 4<sup>th</sup> harmonic is shown to be quite independent of the phase or amplitude imbalance, and its power level is around -22 dBm since it is the 2<sup>nd</sup> largest even harmonic component. However, owing to the significant frequency difference to the designated main harmonics (i.e., the 2<sup>nd</sup>), the 4<sup>th</sup> harmonic can be well suppressed by a BPF at the output.

#### b) Transformer-Based Balun Structure

Figure 5.2(a) shows a realized layout of the 1:1 TF used in the FM design. Herein, the ultra-thick metal (UTM) layer with  $3\mu\text{m}$  was used for the primary coil, and the two layers below UTM were combined for the secondary coil. Each coil has a center tap to conduct dc-current for the drain or is connected to the bias voltage for the gate. The EM simulation of the transformers was carried out with the HFSS tool.

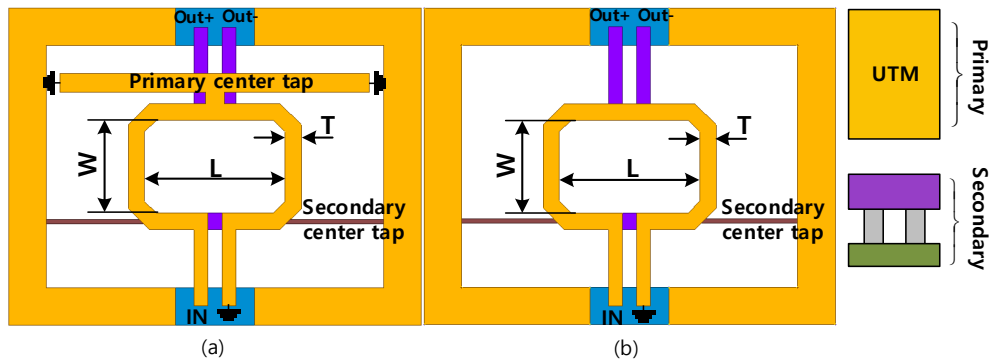


Figure 5.2. HFSS-realization of (a) TF-based balun with AC-grounded primary center tap used in the FM design and (b) a typical TF-based balun.

It is noticed that the primary center tap line in the TF layout is AC-grounded in our design instead of removing this line as in the conventional balun implementation (Figure 5.2(b)). To prove the advantage of the TF structure in Figure 5.2(a) compared to the conventional TF structure in Figure 5.2(b), we compared the two TF structures in terms of efficiency and output balance score at a target frequency, said 20-GHz. The efficiency score was assessed through the maximum available gain ( $G_{ma}$ ) of the balun when it is used as a two-port network to convert the single-ended signal to the differential signal (Figure 5.3(a)). Meanwhile, the output balance score was assessed via the imbalance of  $S_{21}$  and  $S_{31}$  when the two output terminals of the balun are connected to two separated ports (namely port 2 and port 3, and port 1 is the input) (Figure 5.3(b)). For a fair comparison, the baluns are compared in the cases with and without resonant capacitors, which are demonstrated in Figure 5.3(b) and Figure 5.3(c), respectively. The value of resonant capacitors is the imaginary parts of the optimum load and source admittances given in [5.11].

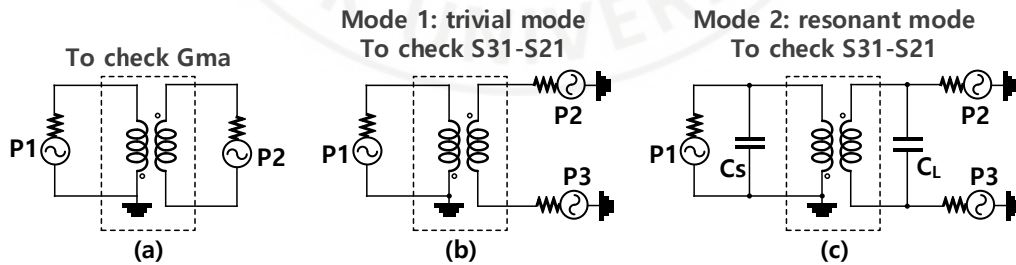


Figure 5.3. Configurations of the TF-based balun (a) the balun is realized as a two-port network to convert the single-ended signal to the differential signal, (b) the three-port network balun without any resonant capacitor, and (c) the three-port balun with resonant capacitors.

The simulations were applied to three TF-based baluns.



1. TF<sub>1</sub> (T, W, L) = (7, 40, 150-um) with AC-grounded primary center tap line (Figure 5.2a). This is the TF in the FM design that works at 20-GHz (FM TF<sub>2</sub>).
2. TF<sub>2</sub> (T, W, L) = (7, 40, 150-um) without AC-grounded primary center tap line (Figure 5.2b).
3. TF<sub>3</sub> (T, W, L) = (7, 40, 60-um) without AC-grounded primary center tap line (Figure 5.2b).

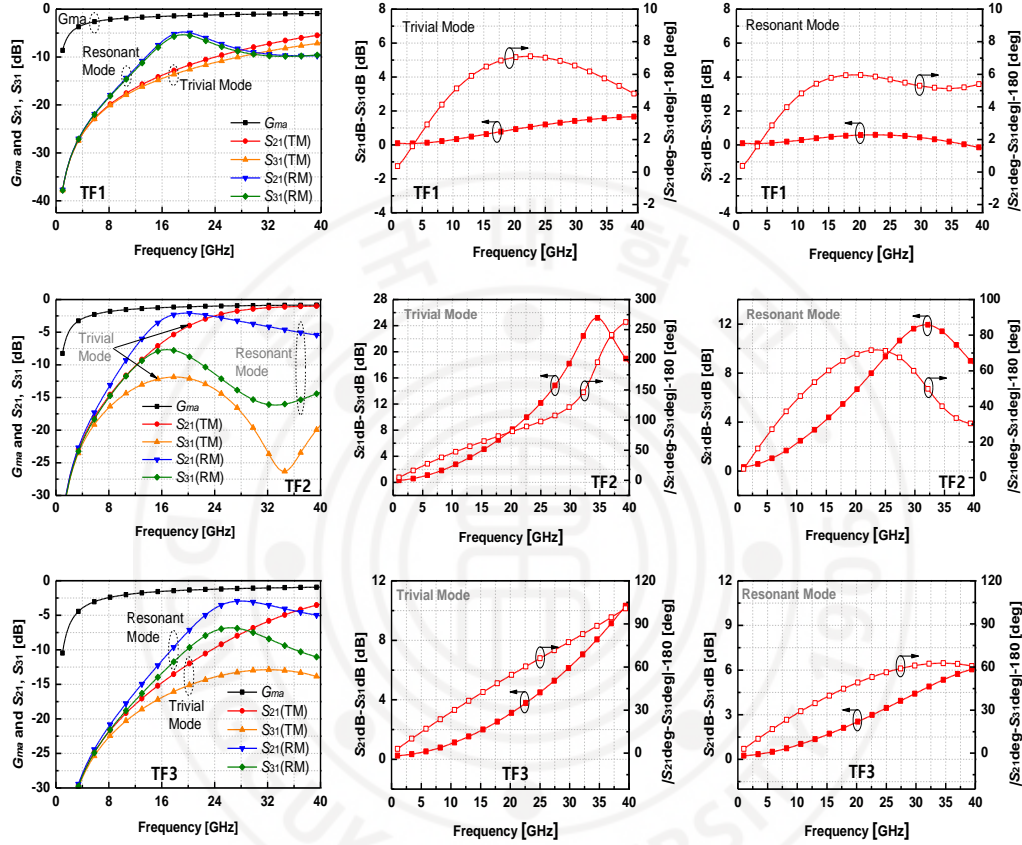


Figure 5.4. Simulated efficiency score ( $G_{ma}$ ) and output balance score ( $S_{21}$ - $S_{31}$ ) of the three TF-based baluns.

The simulation results are shown in Figure 5.4. In the resonant mode, the calculated source and load resonant capacitors ( $C_s$ ,  $C_L$ ) for TF<sub>1</sub>, TF<sub>2</sub>, and TF<sub>3</sub> are (490.2-fF, 181-fF), (209-fF, 110-fF), and (446.4-fF, 276.5-fF) respectively. It can be seen that:

1. The TF-based balun with an AC-grounded primary center tap line (i.e., the structure in Figure 5.2a) achieves a much better output balance score compared to the typical design (the one in Figure 5.2b) even at the same size (TF<sub>1</sub> compared to TF<sub>2</sub>) or at the same efficiency (TF<sub>1</sub> compared to TF<sub>3</sub>).
2. It is noticed that the port impedance of 50-ohm is used in all the ports in the simulation. Therefore, the baluns do not reach their maximum efficiencies in the



resonant mode (i.e.,  $\text{mag}|S_{31}| + \text{mag}|S_{21}| = \text{mag}|G_{ma}|$ ). Also,  $S_{21}$  and  $S_{31}$  do not peak at exactly the target frequency (i.e., 20-GHz). To maximize these gains at the target frequency, the resonant capacitors should be less or more than their globally-optimum values.

The extracted  $G_{ma}$  and the imbalances between  $S_{21}$  and  $S_{31}$  in trivial and resonant modes at 20-GHz are summarized in Table 5.1. In conclusion, it can be seen that the balun structure in Figure 5.2(a) achieves a much better electrical balance at the output compared to the baluns in Figure 5.2(b), even compared to a small size with similar efficiency.

Table 5.1. Efficiency and the imbalance level of the baluns at 20-GHz

TF-based balun	$G_{ma}$ (dB)	Amplitude Imbalance (dB)	Phase Imbalance (deg)
TF <sub>1</sub> : Structure in Fig. 2(a) (T, W, L=7, 40, 150- $\mu\text{m}$ )	-1.337	0.92	7.04
		0.58*	5.96*
TF <sub>2</sub> : Structure in Fig. 2(b) (T, W, L=7, 40, 150- $\mu\text{m}$ )	-1.099	7.98	80.56
		6.57*	69.2*
TF <sub>3</sub> : Structure in Fig. 2(b) (T, W, L=7, 40, 60- $\mu\text{m}$ )	-1.358	3.07	54.06
		2.50*	48.85*

\* In resonant mode

### c) Calculation of the difference of the load capacitors to balance the output voltages

The previous section shows that an implemented balun commonly suffers from output imbalance when the differential-matching capacitors are employed. Therefore, we connected the two output terminals to different load capacitors to mitigate the output imbalance in this work. We deal with the balun as a three-port to calculate the load capacitors, as shown in Figure 5.5. It is noticed that the target of the proposed method is to reduce the imbalance of the voltages on the two output terminals, i.e.,  $V_2$  and  $V_3$ . If the two output ports have the same impedance, this condition is equivalent to balancing  $S_{21}$  and  $S_{31}$ . In the first manuscript, we compared  $Z_{21}$  and  $Z_{31}$  to show the inherent imbalance of the balun. In actual use, the cost function should be the balance of  $V_2$  toward  $V_3$ .

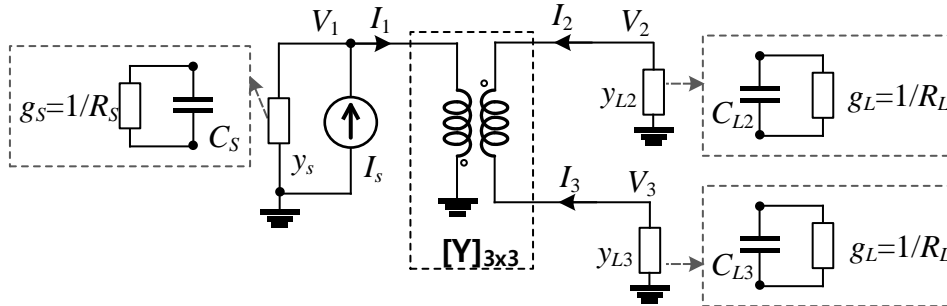


Figure 5.5. Three port network balun with a current source and two load admittance.

In Figure 5.5, the balun's input is excited by a current source  $I_s$  with the source admittance of  $y_s$ . The two output ports are connected with their corresponding load admittances of  $y_{L2}$  and  $y_{L3}$ . The current matrix  $[I]$  of the three-port network is calculated through its  $Y$ -parameter matrix  $-[Y]$  and the voltage matrix  $-[V]$ , as given by

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & y_{13} \\ y_{21} & y_{22} & y_{23} \\ y_{31} & y_{32} & y_{33} \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}.$$

At the three ports, we have:

$$\begin{aligned} I_1 &= I_s - V_1 y_s \\ I_2 &= -V_2 y_{L2} \\ I_3 &= -V_3 y_{L3} \end{aligned}$$

Since the balun is a passive network, its  $Y$ -parameter matrix  $-[Y]$  is symmetric (i.e.,  $[Y]=[Y]^t$ ).

The voltage matrix is rearranged via a matrix  $-[Y_{LS}]$  and  $I_s$  to be

$$\begin{bmatrix} Y_{11} & y_{12} & y_{13} \\ y_{12} & Y_{22} & y_{23} \\ y_{13} & y_{23} & Y_{33} \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} I_s \\ 0 \\ 0 \end{bmatrix},$$

where  $Y_{11}=y_{11}+y_s$ ,  $Y_{22}=y_{22}+y_{L2}$ , and  $Y_{33}=y_{33}+y_{L3}$ .

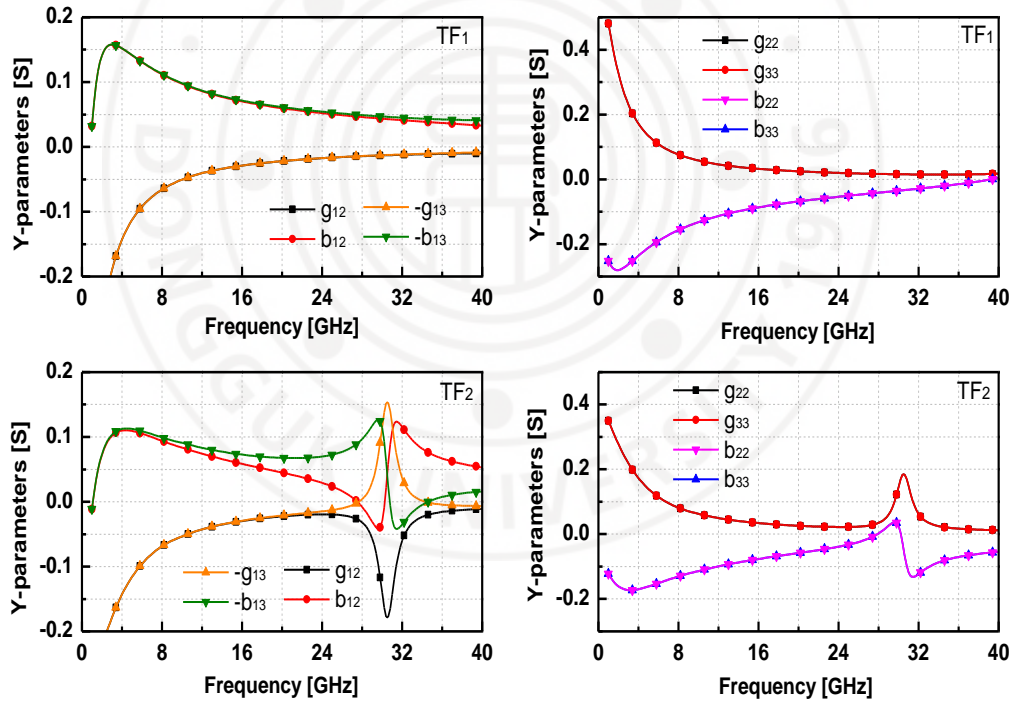
$$\begin{aligned} \Rightarrow \begin{cases} V_2 = \frac{I_s}{\det[\mathbf{Y}_{LS}]} (y_{23}y_{13} - y_{12}Y_{33}) \\ V_3 = \frac{I_s}{\det[\mathbf{Y}_{LS}]} (y_{23}y_{12} - y_{13}Y_{22}) \end{cases} \\ \Rightarrow \frac{V_2}{V_3} = \frac{y_{23}y_{13} - y_{12}Y_{33}}{y_{23}y_{12} - y_{13}Y_{22}} \end{aligned} \quad (5.1)$$

From here, some conclusions can be withdrawn. First, if  $y_{12}=-y_{13}$ , then  $Y_{22}=Y_{33}$  will lead to  $V_2=-V_3$ . It also means that if  $y_{12} \neq -y_{13}$ , then  $Y_{22}$  should be different from  $Y_{33}$  to minimize the imbalance between  $V_2$  and  $V_3$ . Therefore, the imbalance between  $y_{12}$  and  $y_{13}$  can characterize the inherent imbalance of the balun. Second, the source admittance does not affect the ratio  $V_2/V_3$ . By contrast, the load admittances affect the ratio  $V_2/V_3$ . To attain  $V_2+V_3=0$ , equation (5.1) yields

$$y_{23}(y_{13} + y_{12}) - (y_{12}Y_{33} + y_{13}Y_{22}) = 0 \quad (5.2)$$

Before further deploying (5.2), some assessments on the  $[Y]$  matrix of the balun are as follows: in a not-strong-unbalanced balun:  $y_{12}$  is quite different from  $-y_{13}$ , but  $y_{22}$  is almost equal to  $y_{33}$  as shown in Figure 5.6. Moreover, the imbalance between  $y_{12}$  and  $y_{13}$  is majorly from their imaginary part, i.e.,  $b_{12}$  and  $b_{13}$ . Herein,  $y_{mn}=g_{mn}+jb_{mn}$  with  $m, n=1\dots3$ . Assuming the quality factors of the load capacitors are high enough so that their conductances are negligible, then we have  $G_L=G_{22}=G_{33}=g_{22}+g_L=g_{33}+g_L$ , where  $g_L$  is the conductance of the port (or the gate of the doubler in the real case). In summary, we can assume the following conditions

- 1)  $G_{22} = G_{33} = G_L$
- 2)  $g_{12} \approx -g_{13}$
- 3)  $\Delta b_{23} = b_{12} + b_{13} \ll b_{12}, b_{13}$
- 4)  $y_{22} = y_{33}$



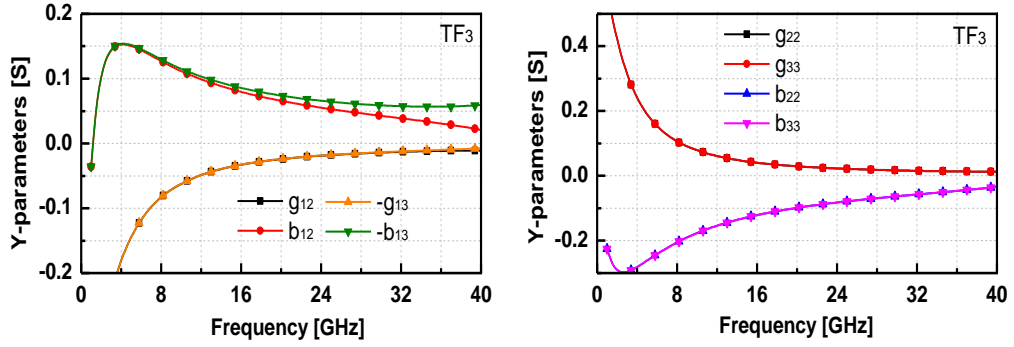


Figure 5.6. Extracted Y-parameters of TF1 (slightly unbalanced), TF2 (strongly unbalanced), and TF3 (unbalanced).

Intuitively, because when  $y_{12}+y_{13}=0$ ,  $B_{33} = B_{22}$  is the solution of  $V_2=-V_3$ , it is also expected that  $B_{33}$  is slightly different from  $B_{22}$  when  $y_{12}+y_{13}$  is somewhat different from 0. Under the conditions in (5.3), equation (5.2) leads to

$$\begin{cases} B_{33} - B_{22} = \frac{\Delta b_{23}}{b_{12}} (b_{23} - B_{22}) \\ G_L = g_{23} - \frac{g_{12}}{b_{12}} (b_{23} - B_{22}) \end{cases} \quad (5.4)$$

In a real case, the value of  $B_L$  ( $B_L=B_{22}\approx B_{33}$ ) should be specified from maximizing power transfer for the balun, and  $G_L$  is un-designable due to the specific conductance of the gates the balun is connected to. Therefore, the imbalance between  $V_2$  and  $V_3$  could be mitigated by differentiating the load capacitors in port 2 and port 3 of the balun, and their difference is estimated to be

$$C_{L3} - C_{L2} = \frac{\Delta b_{23}}{\omega b_{12}} (b_{23} - B_{22}) = \frac{b_{12} + b_{13}}{\omega b_{12}} (b_{23} - B_{22}), \quad (5.5)$$

where  $\omega$  is the angular frequency.

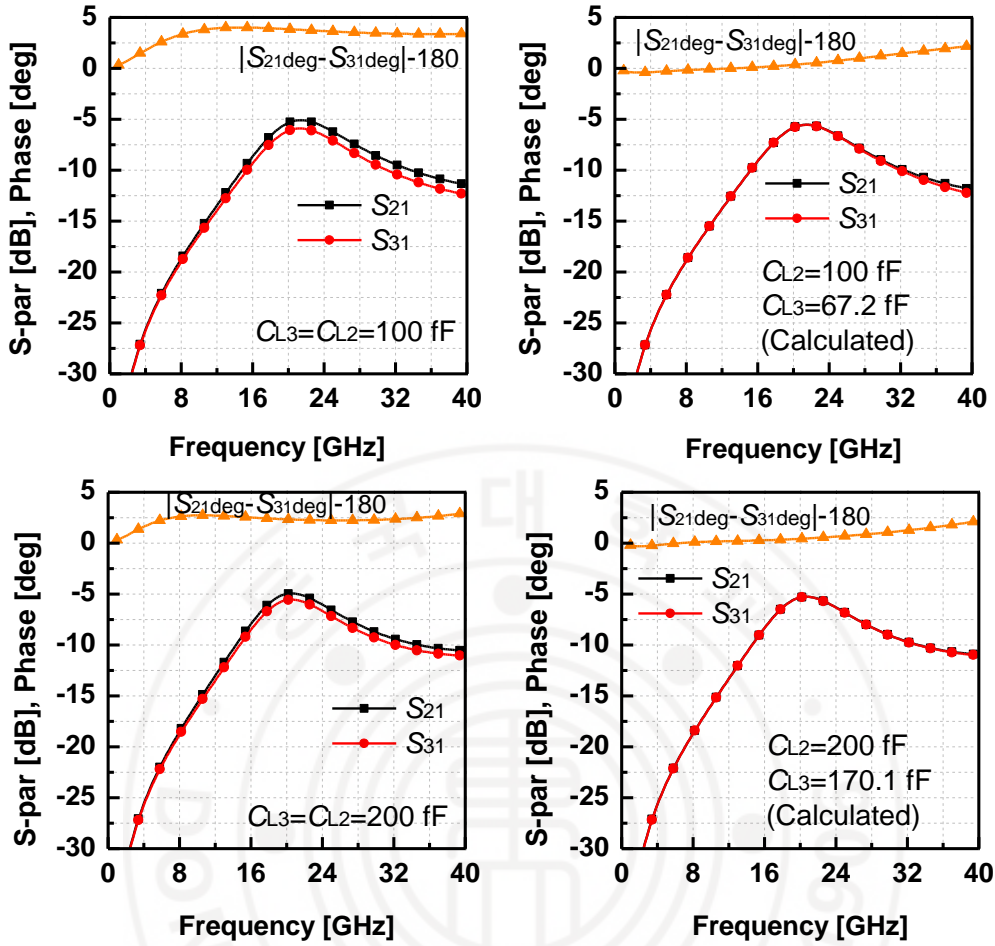


Figure 5.7. Simulated  $S_{21}$  and  $S_{31}$  of TF1 at  $C_{L2}=100$ -fF and  $200$ -fF in the cases of  $C_{L3}=C_{L2}$  and calculated from (5.5).

To evaluate the effectiveness of the formula (5.5), we compared  $S_{21}$  and  $S_{31}$  of the balun in the cases of using  $C_{L3}=C_{L2}$  and using  $C_{L3}$  calculated from (5.5). The value of  $C_{L2}$  was chosen arbitrarily, and the source capacitance in the resonant mode was used. For the TF<sub>1</sub>, if  $C_{L2}=100$ -fF or  $200$ -fF,  $C_{L3}$  is calculated to be  $67.2$  fF and  $170.1$ -fF, respectively. Figure 5.7 shows the simulated  $S_{21}$  and  $S_{31}$  of the TF<sub>1</sub> at  $C_{L2}=100$ -fF and  $200$ -fF. As observed, the formula (5.5) provides a good estimation of the difference between  $C_{L2}$  and  $C_{L3}$  to balance the output voltages. For further investigation, we applied similar simulations for TF<sub>2</sub> and TF<sub>3</sub> at  $C_{L2}=200$ -fF, and the simulation results are shown in Figure 5.8. In the case of TF<sub>2</sub> which is strongly unbalanced, the calculated  $C_{L3}$  is  $-267$ -fF when  $C_{L2}=200$ -fF. This means an inductor is required at port 3. However, an un-physical capacitor with a negative capacitance was still used for mathematical verification. As can be seen, the formula (5.5)

is still useful when applying for unbalanced baluns like TF<sub>2</sub> and TF<sub>3</sub>. From Figure 5.7, it also can be seen that under the source resonant condition, the peaking frequency of S<sub>21</sub> and S<sub>31</sub> does not change much when the load capacitor C<sub>L2</sub> changes from 100-fF to 200-fF.

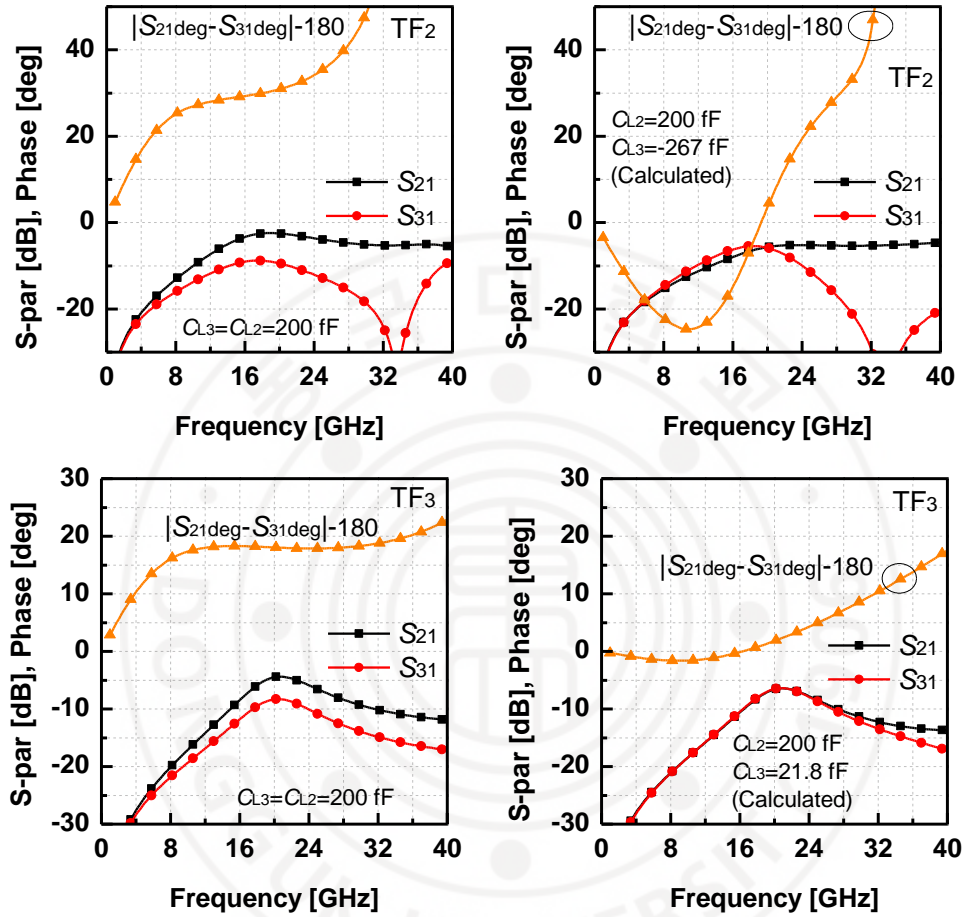


Figure 5.8. Simulated S<sub>21</sub> and S<sub>31</sub> of TF<sub>2</sub> and TF<sub>3</sub> at C<sub>L2</sub>=200-fF in the case of C<sub>L3</sub>=C<sub>L2</sub> and the case C<sub>L3</sub> calculated from (5.5).

d) Calculation of the load capacitors to maximize the power transfer

Assuming that we achieve the voltage balance at the balun output, i.e., V<sub>2</sub>=-V<sub>3</sub>, the efficiency of the balun is calculated by using

$$\eta = \frac{P_{out}}{P_{in}} = \frac{-\frac{1}{2} \operatorname{Re}(V_2 I_2^*) - \frac{1}{2} \operatorname{Re}(V_3 I_3^*)}{\frac{1}{2} \operatorname{Re}(V_1 I_1^*)} = \frac{-\frac{1}{2} \operatorname{Re}(V_2 (I_2 - I_3)^*)}{\frac{1}{2} \operatorname{Re}(V_1 I_1^*)}$$



The calculation of  $P_{out}$  is the power flowing to the equivalent output port with a port voltage of  $V_{2e}=V_2$  and a port current of  $I_{2e}=I_2-I_3$ . The formula for the port voltages  $[V]$ , and current  $[I]$  using a Y-parameter matrix  $[Y]$  is rearranged as follows

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & y_{13} \\ y_{21} & y_{22} & y_{23} \\ y_{31} & y_{32} & y_{33} \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \Rightarrow \begin{bmatrix} I_{1e} \\ I_{2e} \end{bmatrix} = \begin{bmatrix} y_{11e} & y_{12e} \\ y_{21e} & y_{22e} \end{bmatrix} \times \begin{bmatrix} V_{1e} \\ V_{2e} \end{bmatrix} \quad (5.6)$$

where

$$\begin{aligned} y_{11e} &= y_{11} \\ y_{12e} &= y_{12} - y_{13} \\ y_{21e} &= y_{21} - y_{31} \\ y_{22e} &= y_{22} - y_{23} + y_{33} - y_{32} \end{aligned} \quad (5.7)$$

Equations (5.6) and (5.7) represents the relationship between the currents and voltages in a two-port network in which one port has a voltage of  $V_{1e}=V_1$  and a current of  $I_{1e}=I_1$  while the other has a voltage of  $V_{2e} = V_2$  and a current of  $I_{2e} = I_2-I_3$ , as shown in Figure 5.9.

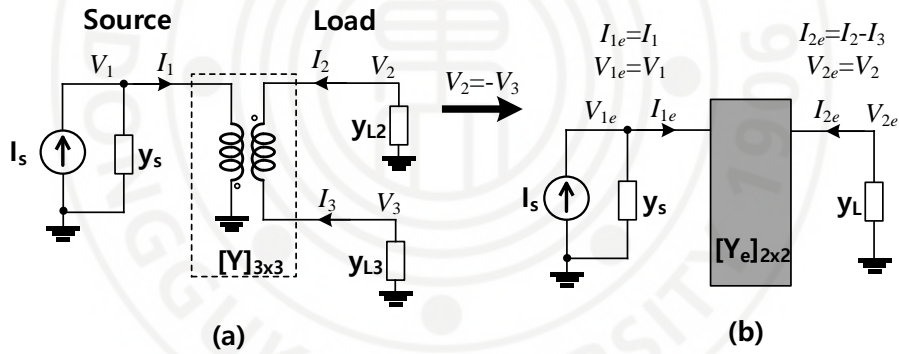


Figure 5.9. Equivalent two-port network of a balun.

The optimal source ( $Z_{Sopt}$ ) and load ( $Z_{Lopt}$ ) and for the equivalent two-port network in Figure 5.9(b) are respectively given by [5.10] as below

$$\begin{aligned} Z_{Sopt} &= Y_{Sopt}^{-1} = r_{11}(\theta_r + j\theta_x) - jx_{11} \\ Z_{Lopt} &= Y_{Lopt}^{-1} = r_{22}(\theta_r + j\theta_x) - jx_{22} \end{aligned} \quad (5.8)$$

with parameters

$$r_c = \text{Re}\left\{\sqrt{Z_{12}Z_{21}}\right\}; \quad x_c = \text{Im}\left\{\sqrt{Z_{12}Z_{21}}\right\}$$

$$\theta_r = \sqrt{\left(1 - \frac{r_c^2}{r_{11}r_{22}}\right)\left(1 + \frac{x_c^2}{r_{11}r_{22}}\right)}$$

$$\theta_x = \frac{r_c x_c}{r_{11}r_{22}},$$

where  $Z_{ij}=r_{ij}+jx_{ij}$  ( $i,j=1,2$ ) are matrix elements of the  $Z$ -matrix. On the output side, the output admittance of the equivalent two-port network can be calculated as

$$y_{oute} = \frac{I_{2e}}{V_{2e}} = \frac{I_2 - I_3}{V_2} = \frac{I_2}{V_2} + \frac{I_3}{V_3} = y_{out2} + y_{out3}$$

Hence, the optimum load capacitors can be calculated by

$$\begin{aligned} \Rightarrow Y_{Lopt} &= y_{oute}^* = (y_{out2} + y_{out3})^* = (Y_{L2opt} + Y_{L3opt}) \\ \Rightarrow C_{L2opt} + C_{L3opt} &= \frac{\text{Im}(Y_{Lopt})}{\omega} \end{aligned} \quad (5.9)$$

From equations (5.5) and (5.9), we can easily calculate the value of  $C_{L2}$  and  $C_{L3}$ . Since  $g_{L2}=g_{L3}=g_L$ , the load conductance is calculated by

$$\Rightarrow g_L = \frac{\text{Re}(Y_{Lopt})}{2} \quad (5.10)$$

It is noteworthy that the single-ended-to-differential two-port configuration of a balun can be derived from its three-port network (Figure 5.9(a)) under the conditions of  $I_2=-I_3$  and  $V_{port2}=V_2-V_3$ , which are different from the equivalent two-port in Figure 5.9(b) with the conditions of  $V_2=-V_3$  and  $I_{port2}=I_2-I_3$ . However, if the balun is perfectly symmetric, the two methods would result in the same optimum source impedance and two electrically-equivalent load impedance. For instance, the single-ended-to-differential two-port of the TF<sub>1</sub> has the optimum load and source admittance of  $Y_{s\_opt1}=27+j61.6$  (mS) and  $Y_{L\_opt1}=26.8+j22.8$  (mS). Meanwhile, the equivalent two-port of the TF<sub>1</sub> in Figure 5.9(b) has the optimum load and source admittance of  $Y_{s\_opt2}=27+j61.5$  (mS) ( $\approx Y_{s\_opt1}$ ) and  $Y_{L\_opt2}=107.2+j91$  (mS) ( $\approx 4Y_{L\_opt1}$ ) which is just slightly different from the former one. From (5.5) and (5.8), the optimum capacitances for the two output terminals were calculated to be  $C_{L2\_opt}=374.7$ -fF and  $C_{L3\_opt}=349.8$ -fF.

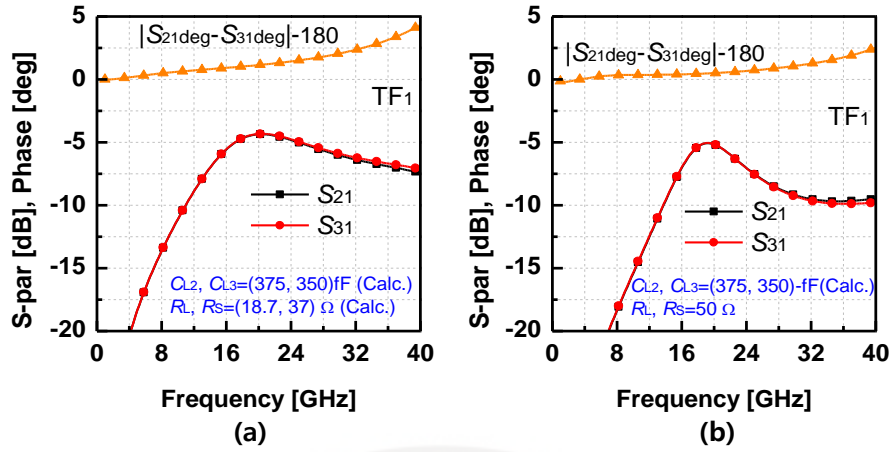


Figure 5.10. Simulated  $S_{21}$  and  $S_{31}$  of TF1 at (a) the optimum load and source admittances and (b) with optimum load and source capacitances, and 50- $\Omega$  load and source impedances.

In conclusion, the optimum load and source impedance of the three-port balun can be calculated from four equations (5.5), (5.8), (5.9), and (5.10). The simulated conversion gains,  $S_{21}$  and  $S_{31}$ , of TF1 under the optimum source ( $R_S=37\text{-ohm}$ ,  $C_S=489.4\text{-fF}$ ) and load impedances ( $R_L=18.7 \Omega$ ,  $C_{L2}=374.7 \text{ fF}$ ,  $C_{L3}=349.8 \text{ fF}$ ) which are calculated by (5.5) and (5.8)-(5.10) are shown in Figure 5.10(a). As can be seen,  $S_{21}$  and  $S_{31}$  peak at 20-GHz with a maximum gain of -4.33 dB, which is corresponded well with the simulated  $G_{ma}$  of -1.33 dB. The simulation was performed again (Figure 5.10(b)) with the typical 50- $\Omega$  load and source impedances as we did in Figure 5.7. Compared to the cases of  $C_L=100\text{-fF}$  or  $200\text{-fF}$ , the calculated optimum load capacitances provide an insignificant difference in the conversion gains in terms of the peak value and the peak frequency.

### 5.2.2 Eight-time frequency multiplier design

The entire schematic diagram of the proposed W-band eight-time frequency multiplier (x8 FM) is illustrated in Figure 5.11. The FM comprises three PPDs operating at the output center frequencies of 20, 40, and 80 GHz, respectively, and each PPD is followed by its corresponding driving amplifiers (DAs).

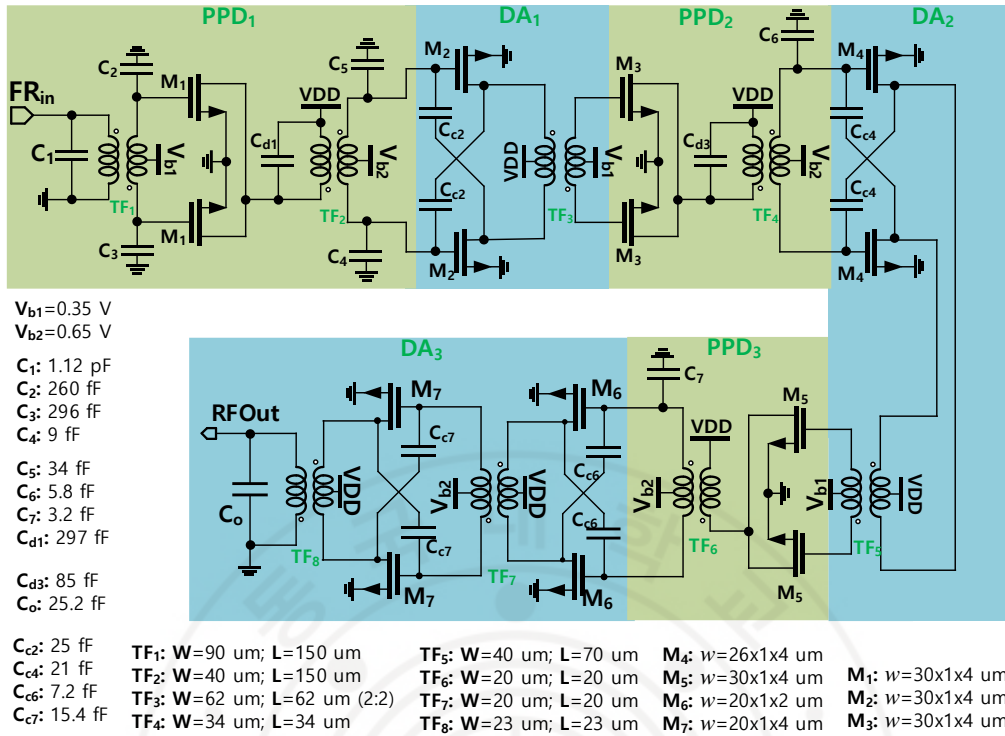


Figure 5.11. Schematic of the  $\times 8$  frequency multiplier.

a) Push-push frequency doublers

The first doubler is composed of a 10 GHz front balun ( $TF_1$ ) to convert the single-ended input signal into a balanced output; a push-push differential pair was used to perform frequency multiplication, and an output balun ( $TF_2$ ) was employed to generate the differential output signal. As stated, any poor sinusoidal signal from the input side would be more distorted toward the output. The doublers in the FM should provide a good harmonic rejection to spurs to improve overall HRR performance. This is particularly important for the first doubler since it determines the power levels of the two vicinity harmonics around the main tone at the output (i.e., the 7<sup>th</sup> and the 9<sup>th</sup> tones in  $\times 8$  FM), which typically dominate the HRR performance of the whole FM. The 7<sup>th</sup> and the 9<sup>th</sup> tones are mainly generated from the mixed harmonics with the fundamental signal of the input.

The first doubler works at a relatively low input frequency of 10-GHz, allowing the input balun to use a 2:2 TF to save the area with a good conversion gain. However, a 2:2 TF has a relatively poor output balance. Therefore, a large 1:1 TF ( $W=90\text{-}\mu\text{m}$ ;  $L=150\text{-}\mu\text{m}$ ) was used to implement the front balun with a better signal balance. The proposed method using two separated capacitors connected to each output terminal of the balun was employed. One advantage of using parallel matching capacitors for the balun is that the gate and drain

parasitics of the active devices can be absorbed into the calculated capacitance values for the baluns with inductive TF. For TF<sub>1</sub>, the load capacitances after excluding these gate parasitics were calculated to be 260-fF and 296-fF for positive and negative terminals of the differential pair, respectively. An electromagnetic (EM) simulation carried out for the 3D model of the TF<sub>1</sub> in HFSS showed a conversion gain of -3 dB and phase and amplitude imbalances of 0.4° and 0.03 dB at 10-GHz, respectively, as shown in Figure 5.12. Similarly, there are three capacitors of  $C_{d1}$ =297-fF,  $C_4$ =9-fF, and  $C_5$ =34-fF, which are involved in the impedance matching and balancing for the output balun (TF<sub>2</sub>) of the first doubler.

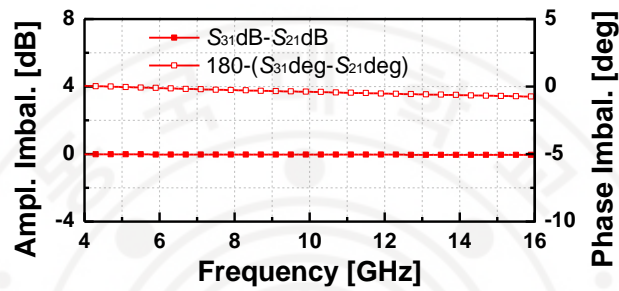


Figure 5.12. Simulated amplitude and phase imbalances of the first balun (TF<sub>1</sub>).

Since the parasitic capacitance at the gate and drain of an active device is non-linear, and their instantaneous values depend on the signal level, the device size of each doubler was designed considering the trade-off between the conversion gain and the harmonic rejection performance. MOS transistors with the size of 120- $\mu$ m were used for the three doublers in this work (i.e., M<sub>1</sub>, M<sub>3</sub>, and M<sub>5</sub>). For the first doubler working at 20 GHz, the width of 120- $\mu$ m is relatively small, and its parasitic capacitance is insignificant compared to its surround matching capacitors of  $C_2$ ,  $C_3$ , and  $C_{d1}$ . For the third doubler operating at 80 GHz, the width of 120- $\mu$ m is considered relatively large to enhance the output power. At the output stage, the HRR performance is less important than the first stage since its fundamental frequency is  $4f_0$ , which can be easily filtered out by the corresponding DA.

Meanwhile, the output power criterion is more important for the third doubler because it directly determines the saturated output power of the whole FM. Therefore, in this design, a small TF (TF<sub>6</sub>:  $W=L=20$ - $\mu$ m) with an acceptable coupling factor was used at the output of the third doubler so that its primary inductance can resonate out the drain's parasitic capacitance without incurring any additional capacitor.

Figure 5.13(a) shows the output power of the first doubler versus the input power. It is shown that the output power of the  $2f_0$  harmonic increases almost linearly as the increase of input power until the saturation of the output power. The conversion gain of the first doubler is around -8 dB, i.e., -5 dB, excluding the insertion loss of the input balun. However, the doubler should be avoided to be driven into the saturated region due to a poor rejection level for the 4<sup>th</sup> harmonic, which would degrade the overall HRR performance of the FM. Instead, the doubler was designed to operate with an average input power for better HRR performance. The proper amount of the output power in driving the next stage PPD was provided by the DA after the doubler.

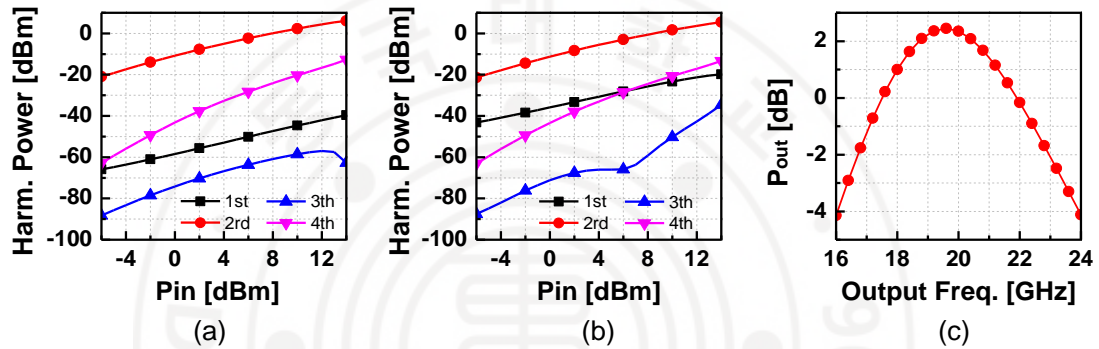


Figure 5.13. The simulated power level of several harmonics of the first doubler at 10-GHz: (a) the original design using the proposed method to balance the baluns; (b) using differentially-connected capacitors for the baluns.

Owing to the balancing circuit with two separate load capacitors for the baluns, the 1<sup>st</sup> and 3<sup>rd</sup> tones are much smaller than the 4<sup>th</sup> tone which dramatically improves the overall HRR performance. To illustrate the advantage of the proposed technique, we simulated the output power of the first doubler but with the typical single matching capacitor connected differentially as in Fig. 4(a). The simulation results are shown in Figure 5.13(b). As can be observed, while the power levels of the even harmonics (2<sup>nd</sup> and 4<sup>th</sup> tones) are almost the same as the original design, the odd tones increase significantly compared to their counterparts in Figure 5.13(a). This improvement is more meaningful since the harmonics ( $6f_0$ ,  $7f_0$ ,  $9f_0$ ,  $10f_0$ ) vicinity to the output frequency ( $8f_0$ ) are more difficult to be filtered. The second and the third doublers have the same configuration as the first doubler. The size of the output baluns of each PPD is maximized to achieve better coupling factors to optimize the conversion gain at each working frequency. Thus, the capacitive load at one terminal



could be fully absorbed by the gate parasitics of the DA for the second and third PPDs. The simulated output power of the second and the third doublers are presented in Figure 5.14 and Figure 5.15, respectively. From the first to the third doubler, the conversion gains and their output powers are gradually reduced because of the degradation of  $G_m$  at a higher frequency for the same transistor size.

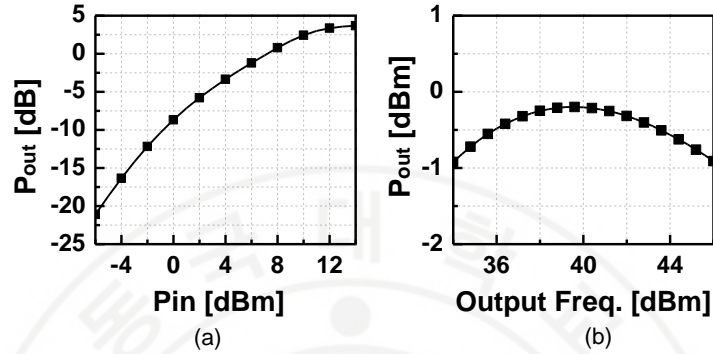


Figure 5.14. Simulated results of the second doubler: (a) Output power ( $P_{out}$ ) versus input power ( $P_{in}$ ) at output frequency  $F_{out}=80$ -GHz; (b)  $P_{out}$  versus  $F_{out}$  at  $P_{in}=7$ -dBm.

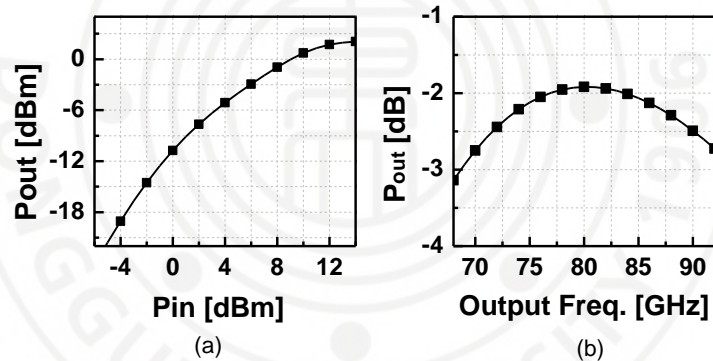


Figure 5.15. Simulated results of the third doubler: (a) Output power ( $P_{out}$ ) versus input power ( $P_{in}$ ) at output frequency  $F_{out}=80$ -GHz; (b)  $P_{out}$  versus  $F_{out}$  at  $P_{in}=7$ -dBm.

#### b) Push-Pull Driving Amplifiers

The DA for the first and second PPD is composed of the single-stage push-pull amplifier (PPA), and it aims to compensate for the conversion loss of the 1<sup>st</sup> and 2<sup>nd</sup> doublers, and they provide specific power levels for the operation of the next doubler. The final DA is designed with two stages of PPAs considering the relatively low  $G_m$  of the active devices at such a high frequency around the E-band. The designed final DA provides the output power of the whole FM larger than 0-dBm. As stated, each push-pull DA also plays as a fourth-order BPF formed by its output matching network with the TF [5.12]. This matching configuration with a TF effectively helps to suppress unwanted high order harmonics generated by the

preceding doublers. The layout of the PPA is well integrated with that of the PPD, which resulted in a compact area occupancy. The metal-oxide-metal (MOM) capacitors ranging from 14-fF to around 80-fF were used considering the higher Q-factor with better design accuracy. Meanwhile, the capacitors larger than 80-fF were implemented with the metal-insulator-metal (MIM) structure. For the capacitor smaller than 14-fF, we manually layout capacitors with Calibre for specifically small capacitances.

*c) HRR performance of the eight-time E-band frequency multiplier*

We simulated the whole FM in HFSS for any TF and signal routing. On simulation, HHR performance is highest at a specific input power range of 5-12 dBm, which makes the main harmonic saturated. The simulated power level of unwanted harmonics versus input frequency at  $P_{in}=10$ -dBm is presented in Figure 5.16(a). More than 33 dBc of the HRR is recorded over the operating frequency ( $f_0$ ) from 8.8 to 11.4 GHz. Owing to the balancing capacitors for TF baluns, the simulated HRR was achieved up to around 55-dBc over a 6.4-GHz bandwidth of the output with  $f_0=9.6$ -10.4 GHz.

To verify the effect of the proposed balancing technique on the whole FM design, a similar simulation was performed for the  $\times 8$  FM with a single shunt capacitor connected differentially to the output of the balun as in the ordinary case. The simulation results of this case are shown in Figure 5.16(b). As observed, the output power of the 7<sup>th</sup> and the 9<sup>th</sup> harmonics dominate the others. The largest HRR is around 45-dBc, which is 10-dB lower than the original  $\times 8$  FM design with the proposed balancing method. Moreover, the 7<sup>th</sup> and 9<sup>th</sup> tones increased quickly as frequency varied from its center, leading to reduced effective bandwidth for a specific HRR performance.

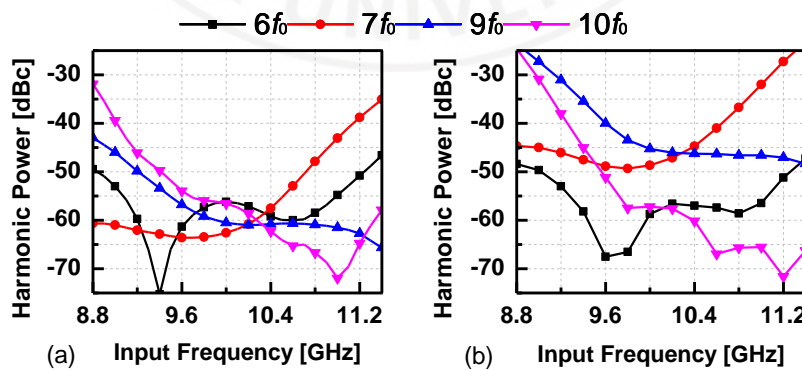


Figure 5.16. Simulated harmonic power of the FM versus input frequency using proposed balancing method (a), and conventional balun (b).

### 5.3 Measurement results

The proposed  $\times 8$  FM was fabricated in 65-nm CMOS process with an occupied area of  $0.95\text{mm}^2$ , including all the pads. Meanwhile, the core FM consumes only  $0.35\text{mm}^2$  showing the advantage of the TF-based push-pull structure. An image of the fabricated E-band  $\times 8$  FM is presented in Figure 5.17. The chip was measured on a probe station using DC and RF probes. The implemented  $\times 8$  FM consumed a DC-current of 164 mA from a 1.2-V supply without an RF input. Figure 5.18 illustrates the measurement setup for the main harmonic power. An X-band signal generator (Agilent 83623B) was used to generate the input signal fed into the  $\times 8$  FM. The output power was measured using a power sensor (W8486a) in combination with a W-band power meter (Agilent E4419B). The connection losses, including cables, probes, and waveguides, were measured and calibrated from the input and output power of the FM.

The output power and conversion gain of the implemented FM versus the input power at various frequencies are presented in Figure 5.19 and Figure 5.20, respectively. The measured output power of the FM increases quickly as the input power increases, and it is saturated at a specific input power level depending on the input frequency due to the limited bandwidth. A peak output power of 0, 5.5, 4.7, and 1.4 dBm is achieved at 8.8, 9.6, 10.4, and 11.2 GHz, which correspond to output frequencies of 70.4, 76.8, 83.2, and 89.6 GHz, respectively. The maximum output power was measured to be 6.3 dBm at the input frequency of  $f_{in}=9.77\text{-GHz}$ . At this input frequency, the  $\times 8$  FM achieved the highest gain of  $-0.4\text{ dB}$  with input power equal to  $4\text{-dBm}$ . At other frequencies, the peak gain is  $-12$ ,  $-2.3$ ,  $-1$ , and  $-5\text{ dB}$  for input frequencies of 8.8, 9.6, 10.4, and 11.2 GHz, respectively.

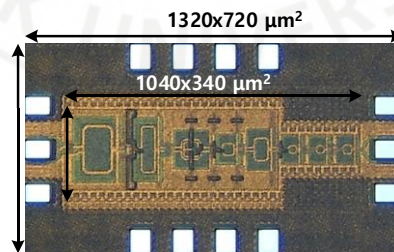


Figure 5.17. Photograph of the  $\times 8$  FM in 65-nm CMOS.

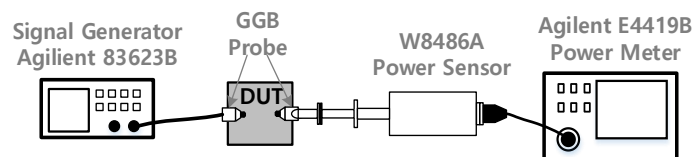


Figure 5.18. Power measurement setup for the main harmonic.

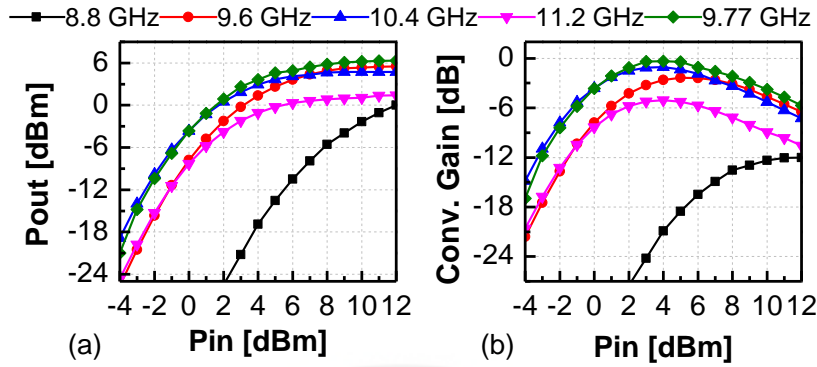


Figure 5.19. (a) Measured output power ( $P_{out}$ ) and (b) measured conversion gain of the  $\times 8$  FM versus input power ( $P_{in}$ ).

The measured output power and efficiency of the  $\times 8$  FM versus output frequency at  $P_{in}=12$  dBm are presented in Figure 5.20. The measured  $P_{out}$  is larger than 0-dBm within the bandwidth of 20.8-GHz, which is from 70.4 to 91.2 GHz. It is noted that the maximum output point with  $f_{in}=9.77$ -GHz is not included in Figure 5.20. Within the measured bandwidth, the efficiency varies from 0.3 to 1.5-%, with the peak value recorded at an output frequency of 78-GHz. Overall, the measured output power and efficiency correspond well with the simulation results. The discrepancy between the measurement and simulation is due to the error from the wideband characterization of the FM and the inaccuracies of the nonlinear component models from the manufacturer.

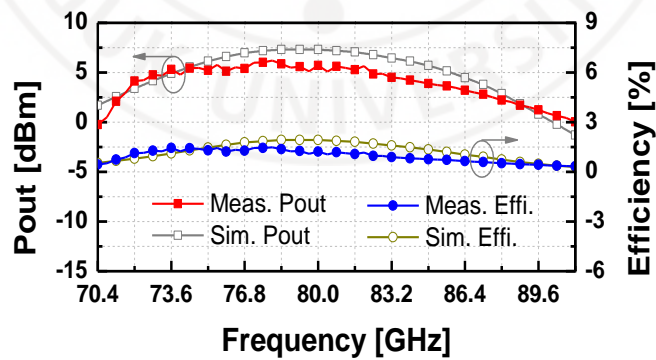


Figure 5.20. Measured output power ( $P_{out}$ ) and efficiency of the  $\times 8$  FM versus output frequency.

The four adjacent undersigned harmonics (i.e., the 6<sup>th</sup>, 7<sup>th</sup>, 9<sup>th</sup>, and 10<sup>th</sup>) cover a wide frequency range. Hence it required two measurement setups for the low and high bands to

measure the spurs as presented in Figure 5.21. A harmonic mixer (Anritsu MA2744A) with the nominal frequency range from 50-75 GHz was used to monitor the harmonics below 75-GHz (Fig. 20(a)), and the harmonics higher than 75-GHz is measured by the harmonic mixer (Agilent 11970W) as shown in Figure 5.20(b). A baseband amplifier was used in the two measurement setups to compensate for the conversion losses of the two harmonic mixers. The losses of the two setups were measured and de-embedded from the results. The measured power level of the 6<sup>th</sup>, 7<sup>th</sup>, 9<sup>th</sup>, and 10<sup>th</sup> harmonics at  $P_{in}=12$  dBm is presented in Figure 5.22. In the operating band, the measured HRR is better than 35-dBc. Particularly, the HRR achieved up to around 50 dBc within an input range from 9.6 to 10.6-GHz, which corresponds to an output frequency bandwidth of 8-GHz from 76.8 to 84.8 GHz. To the best of our knowledge, the implemented  $\times 8$  FM achieved the highest measured HRR compared with other recently reported FMs in similar output bands. Table 5.2 summarizes the performances of the proposed  $\times 8$  FM in comparison with other state-of-arts FM in similar bands. The designed  $\times 8$  FM achieved an excellent bandwidth among other CMOS FMs in this band with a dominating maximum HRR and milliwatt output power levels. Consequently, the FoMs of the FM achieved the highest among other recently reported CMOS FMs in similar working frequencies and comparable to SiGe designs.

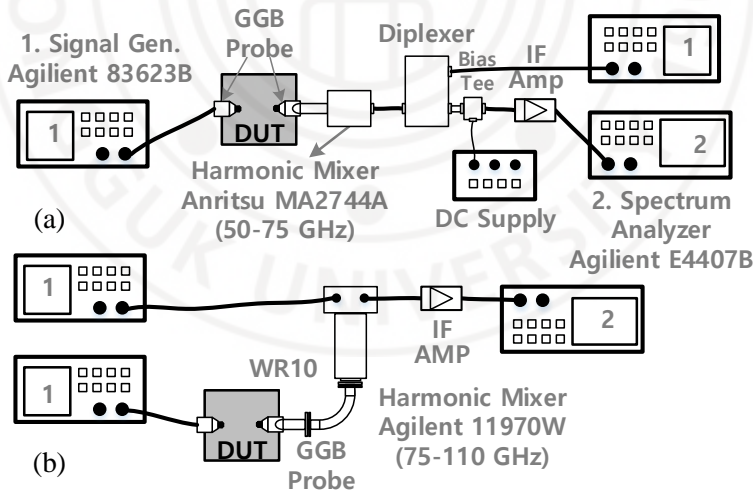


Figure 5.21. Power measurement setup for the 6th, 7th, 9th, and 10th harmonics.



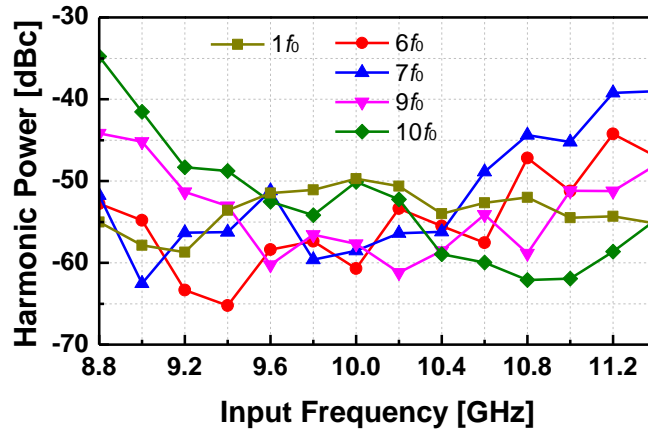


Figure 5.22. Measured output power values at the 1st, 6th, 7th, 9th, and 10th harmonics.

Table 5.2. Comparison of state-of-the-art FMs around W-band

Ref	CMOS Tech.	Freq. (GHz)	3 dB $P_{out}$ BW (%)	MF	$P_{out}$ (dBm)	$P_{dc}$ (mW)	HRR (dBc)	$\eta_{DC}^4$ (%)	Core/Total Area (mm <sup>2</sup> )	FoM
<b>This</b>	<b>65 nm</b>	<b>80/70.4–91.2</b>	<b>18.5</b>	<b>×8</b>	<b>0–6.3</b>	<b>197</b>	<b>35-50</b>	<b>1.4</b>	<b>0.35/0.95</b>	<b>97.0</b>
[5.5]	130 nm	92-102	12.3	×3	-1.5	135	NA	0.6	NA/1.12	NA
[5.6]	65 nm	94/88-99.5	12.2	×9	8.5	438	31-44 <sup>3</sup>	<1.6 <sup>3</sup>	0.26/0.45	92.6
[5.13]	65 nm	77/73-88	19.5 <sup>3</sup>	×2	-8.2 to -3.2	14	19-34 <sup>3</sup>	3.4 <sup>3</sup>	NA/0.23	<65.6
[5.14]	65 nm	74.7-82.2 <sup>2</sup>	NA	×6	0–3.8 <sup>3</sup>	58	NA	NA	NA/1.19	NA
[5.15]	65 nm	77/76.8-78 <sup>2</sup>	1.56 <sup>3</sup>	×6	8.9	117	39	6.6 <sup>3</sup>	NA/1.1	76.5
[5.16]	65 nm	68/57-78	31.3	×3	-2	60	20-30 <sup>3</sup>	<1.1 <sup>3</sup>	NA/0.45	66.1
[5.17]	90 nm	60/51-70	31.6	×3	1.8	44	30-35 <sup>3</sup>	<3.4 <sup>3</sup>	NA/0.92	74.3
[5.18]	40 nm	70/65.6-75.2	13.6	×4	-0.2	11.4	30-40 <sup>3</sup>	8.3	0.1/0.28	75.6
[5.19]	65 nm	94/84-98.4	NA	×8	-7.1	1	10 <sup>3</sup>	19.4 <sup>3</sup>	0.43/0.74	NA
[5.8]	22nm SOI	76/71-81	13.1	×4	3.1	70	35	2.9	0.38/0.52	74.1
[5.20]	45nm SOI	88-104	16.7	×2	10.2	241	NA	4.7 <sup>3</sup>	NA/0.27	NA

1. For two-channel operation when  $P_{out}=0$  dBm, 170 mW for one-channel
2. Synthesizer included
3. Estimated and calculated from figures and tables in the published paper
4.  $\eta_{DC} = P_{out}/P_{dc}$
5.  $FoM(\text{dB}) = P_{out}(\text{dBm}) + \text{HRR}(\text{dBc}) + 10 \log(f_{out}(\text{GHz}) \times \text{MF} \times \text{BW}(\%))$

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## VI. A Sub-THz Amplifier

### 6.1 Gain of transistor and impedance matching for a two-port network

A three-terminal active two-port device (A2P), when working at a small signal domain, can be seen as a linear time-invariant (LTI) two-port network characterized by a matrix of small-signal parameters such as  $Y$ -parameters (or  $S$ - $Z$ - $ABCD$  parameters). Figure 6.1 shows a circuit of a two-port active device (A2P) with its load and source at the input and output respectively.

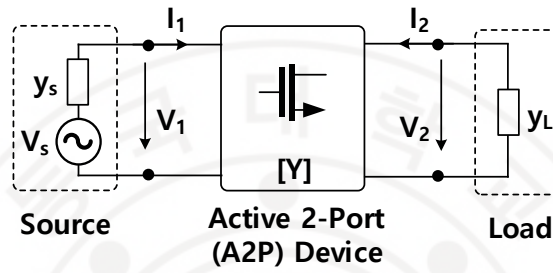


Figure 6.1. An active two-port device with its source and load.

The A2P can amplify the signal from its input to the output with proper load and source matching. Considering both mismatches at the load and the source, *transducer power gain* ( $G_T$ ) is the general figure of merit to assess the gain of the A2P in a system. It is defined as the ratio of power delivered to the load to the power available from the source. When the source and the load impedance are conjugate matched to the input and output port simultaneously,  $G_T$  reaches its maximum value, which is called *maximum available gain* ( $G_{ma}$ ) [6.1]. In [6.1], also shows that the simultaneous matching at the two ports is only possible when the active device is unconditionally stable.  $G_{ma}$  is represented in the form of the stability factor  $K$  as

$$G_{ma} = |A| \left( K - \sqrt{K^2 - 1} \right), \text{ where } A = \frac{Y_{21}}{Y_{12}} = \frac{Z_{21}}{Z_{12}} = \frac{S_{21}}{S_{12}} \quad (6.1)$$

and  $K$  is commonly given in terms of  $Y$ -parameters as:

$$K = \frac{2G_{11}G_{22} - \text{Re}[y_{12}y_{21}]}{|y_{12}y_{21}|}, \quad (6.2)$$

where  $G_{ij}$  and  $B_{ij}$  are conductance and susceptance of  $y_{ij}$ , with  $i, j = 1, 2$  (this notation will be used similarly to other  $y$ -parameters in the thesis). If  $K < 1$ ,  $G_{ma}$  becomes invalid. In this

case, the calculation in (6.1) with  $K=1$ , provides a more meaningful figure of merit, which is called *maximum stable gain* and given as

$$G_{ms} = |A|. \quad (6.3)$$

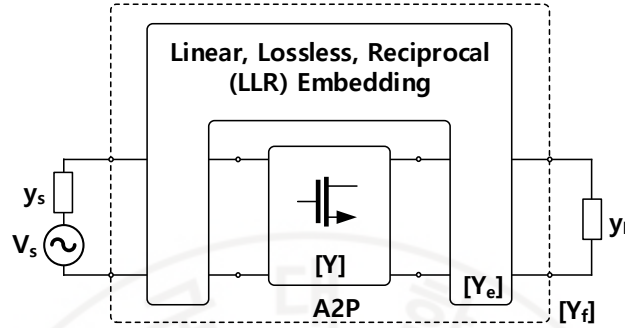


Figure 6.2. An active two-port device is embedded in an LLR network.

By imbedding the A2P into a four-port network, we have a new two-port active network that can possess a higher  $G_{ma}$ . Figure 6.2 depicted a system including an A2P embedded in a linear-lossless-reciprocal (LLR) four-port network with a source and a load on both sides. The small-signal parameters of the embedding network are denoted by letters subscripted with ‘e’ (*i.e.*  $Z_e$ ,  $Y_e$ , or  $S_e$ ); and using ‘f’ for the device after embedding (*i.e.*  $Z_f$ ,  $Y_f$ ,  $S_f$ ).

One arising question is: what is the maximum value of  $G_{ma}$ ? In 1954, Mason introduced a quantity that is invariant under LLR embedding and calculated by [6.2]

$$U = \frac{|y_{12} - y_{21}|^2}{4(G_{11}G_{22} - G_{12}G_{21})}. \quad (6.4)$$

$U$  is equal to the  $G_{ma}$  of an embedded active device that is unilateral, *i.e.*,  $y_{12}=0$ . Therefore, the  $U$  is called *unilateral power gain*. From (6.3),  $G_{ma}$  now can be represented by  $U$ , which is firstly introduced by [6.3] as below:

$$\frac{G_{ma}}{U} = \left| \frac{A - G_{ma}}{A - 1} \right|^2. \quad (6.5)$$

On the edge of unconditional stable, *i.e.*,  $K=1$  [6.3], and when  $A$  is a negative real value [6.3]-[6.4],  $G_{ma}$  will be optimized to the *maximum achievable gain*  $G_{max}$  given by [6.5]:

$$G_{max} = (2U - 1) + 2\sqrt{U(U - 1)}. \quad (6.6)$$

$G_{max}$  is only dependent on  $U$ , and both  $G_{max}$  and  $U$  are inherent characteristics of an A2P. Figure 3 shows all the above-mentioned gains including  $G_{ms}/G_{ma}$ ,  $U$ ,  $G_{max}$ , and  $K$  of an NMOS transistor in a 65-nm process with the size of 32  $\mu\text{m}$ . Because there is still a big gap between  $G_{ms}/G_{ma}$  and  $G_{max}$ , a passive embedding network should be used to exploit fully the gain capability of the NMOS.

The authors in [6.3] introduced a circuit technique, which is later called T-embedding in [6.6], to boost  $G_{ma}$  to  $G_{max}$ , and graphically explained how it works on a coordinate called gain-plane. The T-embedding consists of a parallel passive element connecting the output back to the input and another series of passive elements sinking the common terminal to the ground as shown in Figure 6.2. Continue the work in [6.3], authors in [6.6] provided the analytical solution for the T-embedding.

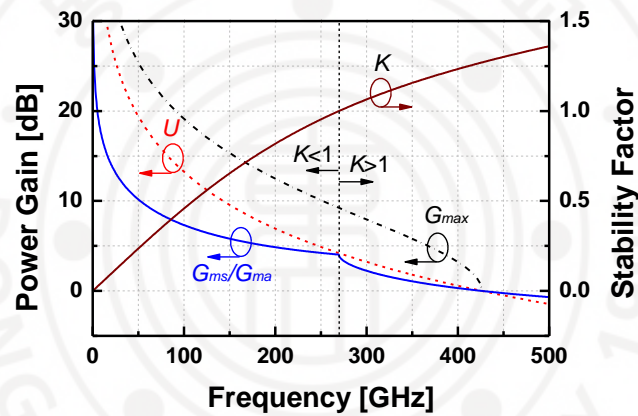


Figure 6.3. Post-layout simulated power gains and stability factor of a 32  $\mu\text{m}$  common source NMOS transistor in a 65 nm CMOS process.

To boost the power transducer gain of an amplifier to its maximum value, *i.e.*  $G_{ma}$ , the primary condition is to perform the impedance matchings at both input and output sides at the same time. This condition is especially important at high frequency due to low gain and low inverse isolation of the active transistors. A general linear time-invariant (LTI) two-port network characterized by a matrix of  $Y$ -parameters (or  $S$ - $Z$  parameters) driven by a general load ( $y_L$ ) and terminated by a general source ( $y_S$ ) is depicted in Figure 6.4.

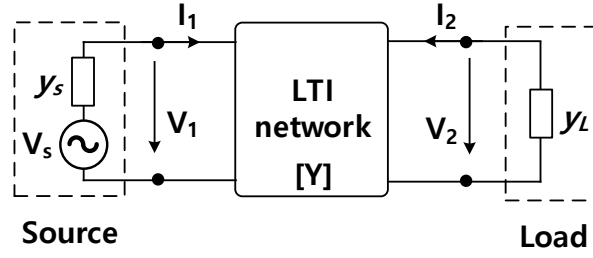


Figure 6.4. An LTI network is connected to a source  $y_s$  and a load  $y_L$ .

The relationship of the voltages  $v_1$ ,  $v_2$  and the currents  $i_1$ ,  $i_2$  in the two ports is

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}, \quad i_2 = -y_L v_2 \quad (6.7)$$

From the above equations, we can calculate the input admittance as

$$y_{in} = \frac{i_1}{v_1} = y_{11} - \frac{y_{12}y_{21}}{y_{22} + y_L} \quad (6.8)$$

Similarly, the output admittance seen from the load toward the network is

$$y_{out} = y_{22} - \frac{y_{12}y_{21}}{y_{11} + y_s} \quad (6.9)$$

The conjugate impedance matching at both sides happens when

$$y_s = y_{in}^*, \quad \text{and} \quad y_L = y_{out}^* \quad (6.10)$$

where “\*” denotes the conjugate. Two constraints in (6.10) for the two variables  $y_s$  and  $y_L$  should lead to one specific solution. As presented in Appendix A, the practical solution of (6.10) is

$$\begin{cases} y_s = \frac{j[\text{Im}(y_{12}y_{21}) - 2G_{22}B_{11}]}{2G_{22}} + \frac{|y_{12}y_{21}|\sqrt{K^2 - 1}}{2|G_{22}|} \\ y_L = \frac{j[\text{Im}(y_{12}y_{21}) - 2G_{11}B_{22}]}{2G_{11}} + \frac{|y_{12}y_{21}|\sqrt{K^2 - 1}}{2|G_{11}|} \end{cases} \quad (6.11)$$

From (6.11), several observations can be made. First, the solution for the problem of conjugated matching impedance at both sides of a two-port network always exists if the ideal source (*i.e.*  $G_s=0$ ) and ideal load (*i.e.*  $G_L=0$ ) are also considered. Second, if  $|K| \leq 1$ , the solution of  $y_s$  and  $y_L$  in (6.11) are purely imaginary. It is also the same for the cases when  $G_{11}$  and/or  $G_{22}$  are zero, as proven in Appendix A. In other words, if the two-port network is potentially unstable, or  $G_{11}$  and/or  $G_{22}$  is zero; the network cannot get conjugate matched



at both sides simultaneously to practical sources and loads (*i.e.*  $G_S > 0$  and  $G_L > 0$ ). The solution in (6.11) shows that boosting the  $G_{ma}$  of a two-port active device to  $G_{max}$  is not the solution to exploiting the full gain capability of the active device. If  $G_{ma}$  was boosted to  $G_{max}$  by using an embedding network, then it requires that the stability factor  $K$  of the embedded active device become unity [6.5]. However, this means we cannot have a practical solution for the problem of conjugate impedance matching at both sides as shown in (6.11). The formula of  $G_{max}$  calculated previously is the upper bound of  $G_{ma}$ .

After considering these above things, it is understood that exploiting fully the gain capability of an active device is more complicated than what was reported previously in the literature. To achieve an effective usage of the gain capability of an active device in the real case, we must:

- (1) Design an embedding network such that the active device after being embedded can have a practical solution of conjugate impedance matching at both sides simultaneously.
- (2) The embedding network should be optimized such that the embedded active device obtains the  $G_{ma}$  as close to  $G_{max}$  as possible.
- (3) The solution of  $y_L$  and  $y_S$  for the embedded active device finally have to be matched to the target impedance which is typically 50  $\Omega$ . Therefore, the loss of the matching networks should be minimized.

The three above criteria are related to each other, for example, to get  $G_{ma}$  close to  $G_{max}$ ,  $K$  should be small, which means the solution of  $y_S$  and  $y_L$  in (6.11) have conductance approaching zeros. This requires high- $Q$  impedance matching networks at the two ports, which may not available in the sub-THz frequency region. In the practical design, the size of the active device should be considered also.

## 6.2. A design of 280-GHz amplifier in SiGe

The schematic of the 280-GHz amplifier is shown in Figure 6.5. Since the  $f_{max}$  of the 130-nm SiGe technology is ~400-GHz, it is possible to achieve gain at 280-GHz. The amplifier is consist of 14 stages of a common emitter amplifier, aiming at a gain of higher than 10-dB at the target frequency. A network constructed from two transmission lines (T-line) and a capacitor is used to perform impedance matchings for one stage of the active device. The device size is chosen by  $2 \times 70 \text{ n} \times 900 \text{ n}$  so that the T-line inductors are long enough for a clear path model for EM simulation. Because the base resistance is around four times lower than the emitter resistance, the series capacitors were used to transform the low

impedance of the base to match the emitter. Large by-pass capacitors using MIM type were used to terminate the T-lines to AC-ground. The base bias currents were connected through average resistors of  $1\text{K}\Omega$ . The amplifier has a chip size of  $710\times 300\text{ }\mu\text{m}^2$  including all the pads.

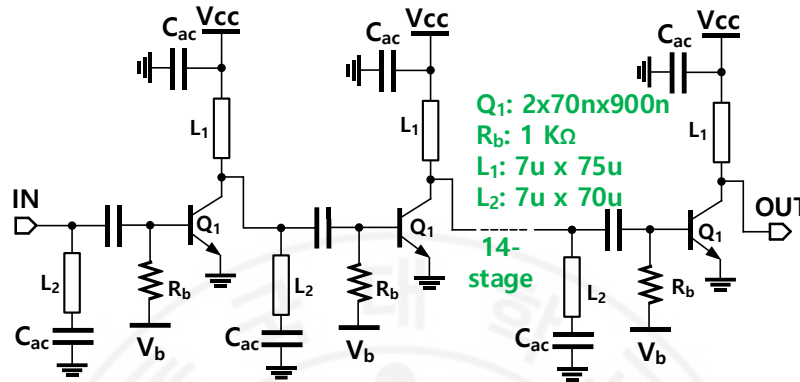


Figure 6.5. Schematic of the 280-GHz amplifier on 130-nm SiGe.

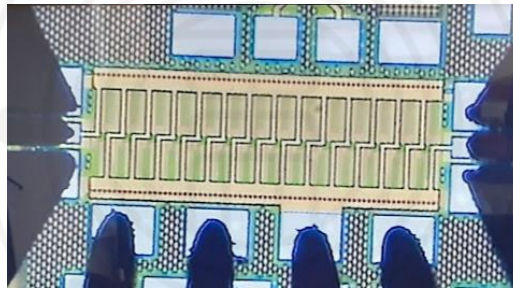


Figure 6.6. A photograph of the 280-GHz amplifier.

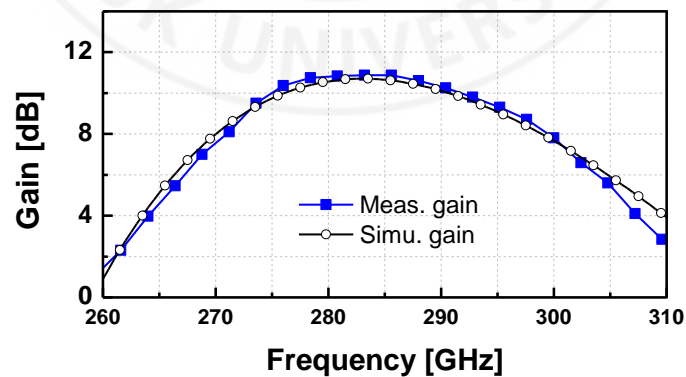


Figure 6.7. Simulated and measured gain of the 280-GHz amplifier.

Figure 6.6 shows a photo of the fabricated amplifier on 130-nm SiGe. The gain of the amplifier is measured by using continuous-wave measurement. This means we injected an input signal into the amplifier and measure its output power. The SGX VDI 2.8 was used to generate the input signal and the power sensor PM5 VDI was used to read the output power. The loss of the waveguide and the GGB probes were calibrated from the measured gain. On measurement, the amplifier achieves a peak gain of 10.8-dBm at 285-GHz with a 3-dB gain bandwidth of 30-GHz from 270-300 GHz. Those measured results correspond well with simulated gain as shown in Figure 6.7. The amplifier is measured to have a peak output power of 0-dBm recorded at 274-GHz.

### 6.3 A design of 280-GHz receiver in SiGe

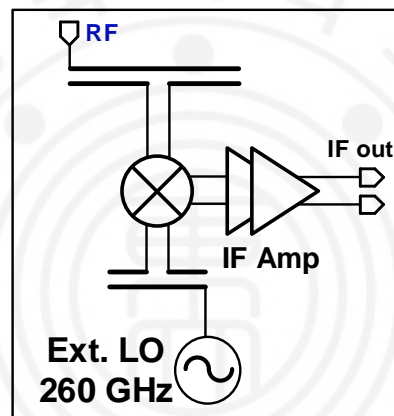


Figure 6.8. Block diagram of the 280-GHz receiver.

Figure 6.8 shows the block diagram of the mixer-first receiver designed on a 130-nm SiGe technology. The receiver consists of a mixer to down-convert the RF input signal from 260-300 GHz to the IF signal by mixing it with an external LO source of 259-GHz. An IF amplifier was used to amplify the IF signal at the output. The schematic of the mixer is presented in Figure 6.9. Double balanced mixer structure was used to mitigate the leakages from the three ports to each other and improve the linearity compared to the single-balanced mixer.

The  $V_{cc}$  is fed via resistors to achieve wideband impedance matching to the input of the IF amplifier. Also, the output of the mixer is directly connected to the input of the IF amplifier with the aimed bias voltage for a normal operation of the IF amplifier. The NMOS was used to conduct the tail current to achieve a compact layout. It is noticed that the tail

NMOS plays as a current mirror to ensure the differential mixing operation. In the RF path, a T-line inductor is used to resonate the parasitic capacitances at the bases. On simulation, the mixer achieves a peak gain of -9 dB and the variation is on 1-dB in the operation band. The single-sideband noise figure (NF) is 16-17 dB. The presented  $S_{22}$  is matched to the high impedance input of the IF amplifier rather than 50-ohm in the typical setup.

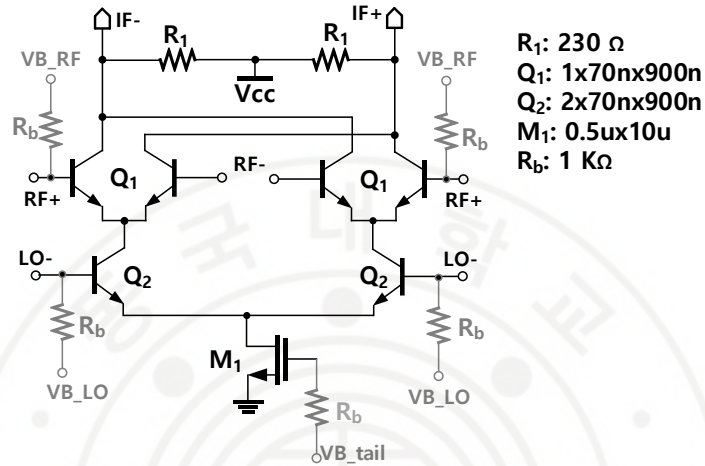


Figure 6.9. Schematic of the mixer in the 280-GHz Rx.

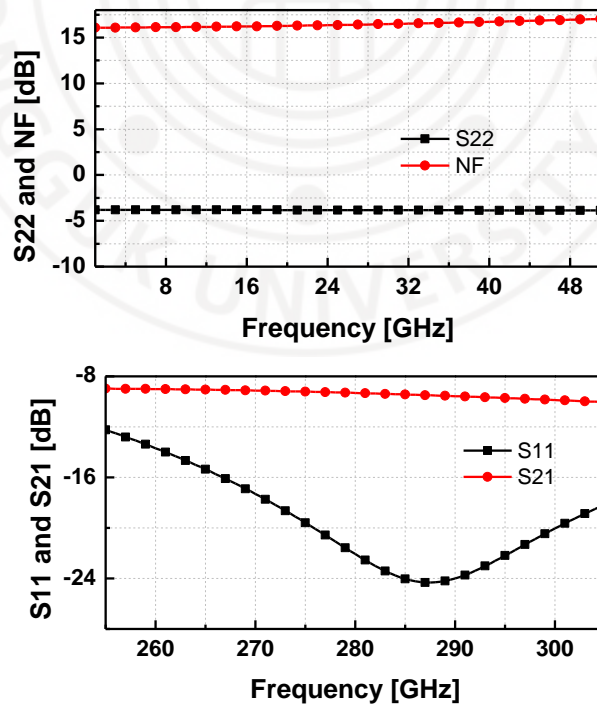


Figure 6.10. Simulated gain and NF of the mixer.

Figure 6.11 shows the schematic of the IF amplifier. The differential IF amplifier is designed using the inductive peaking technique to achieve a wideband operation. In this structure, an inductor is connected in series with a resistor to conduct the emitter current for the transistor. In this way, the high inductance of the inductor could compensate for the parasitic capacitance at the emitter at a high frequency. In the low-frequency region, the series resistor plays as the main impedance matching element. Different inductance and resistance values at the four stages were used to flatten the gain. Since the inductors do not require high-quality factors, they can be implemented with low metal layers to save the area. It is noticed that the bias current to the bases was done by using  $1\text{K}\Omega$  resistors. On simulation, the IF amplifier consumes a current of  $40.3\text{ mA}$  from a  $2.3\text{-V}$  voltage supply. It achieves a gain of  $35\text{-dB}$  as shown in Figure 6.12. It is noticed that the gain at low frequency was equalized to compensate for the trend of the mixer with a better conversion loss at the low frequency. The IF amplifier attains a good impedance matching on the load side when S22 is smaller than  $-10\text{ dB}$  from  $1\text{-}60\text{ GHz}$ . The simulated NF is between  $3.2$  and  $4.7\text{ dB}$  in the target band.

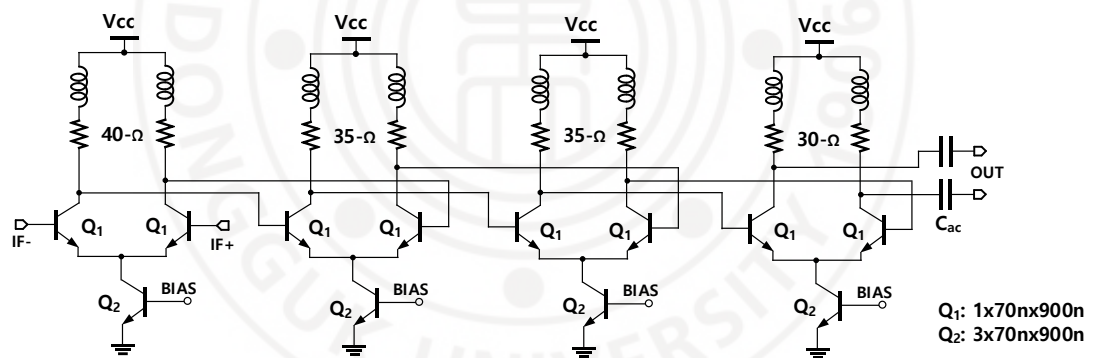


Figure 6.10. Schematic of the IF amplifier in the 280-GHz receiver.

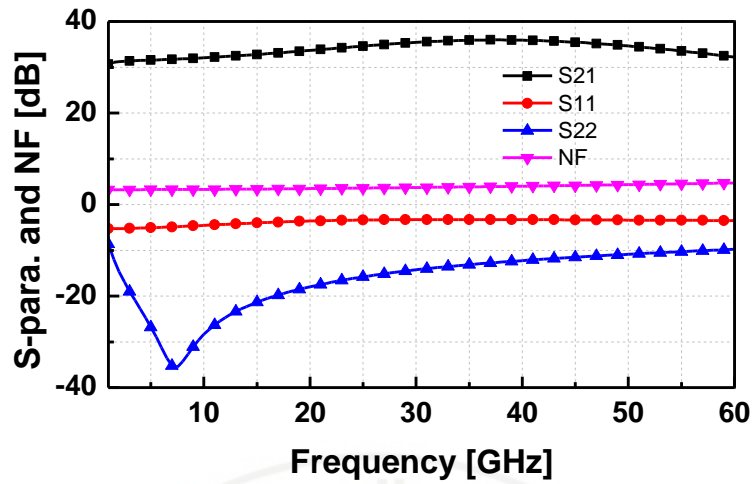


Figure 6.11. Simulated S-parameters and NF of the IF amplifier.

At frequencies around 280-GHz, it is difficult to implement an inductive transformer as a balun due to its low SRF. Therefore, the balun for the RF and LO inputs were implemented based on the Marchand type. Figure 6.12 shows an HFSS implementation of the balun for the RF input. The Marchand balun was implemented using the top metal layer to minimize the insertion loss which is simulated around 1.1 dB as be shown in Figure 6.13.

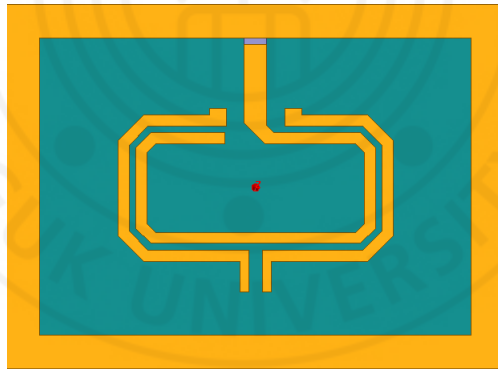


Figure 6.12. HFSS implementation of the Marchand balun at RF input.



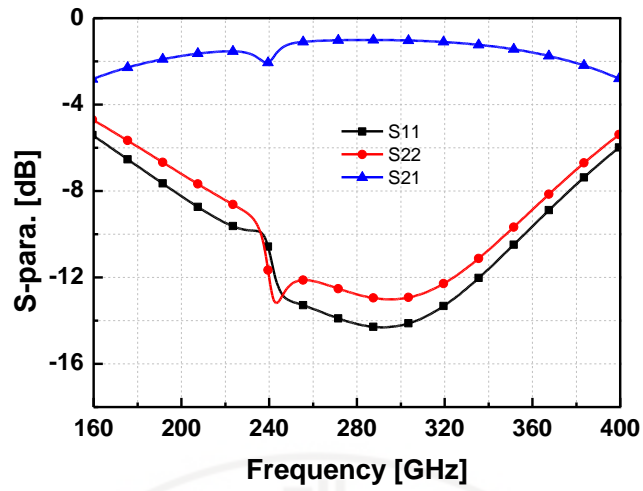


Figure 6.13. Simulated S-parameters of the RF balun.

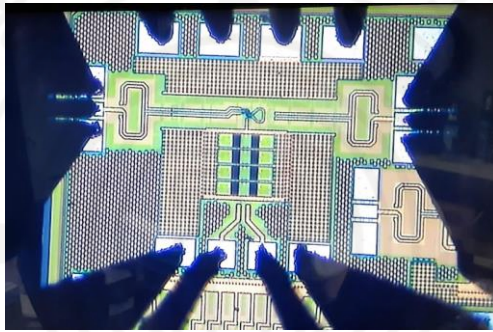


Figure 6.14. A photograph of the measured 280-GHz receiver.

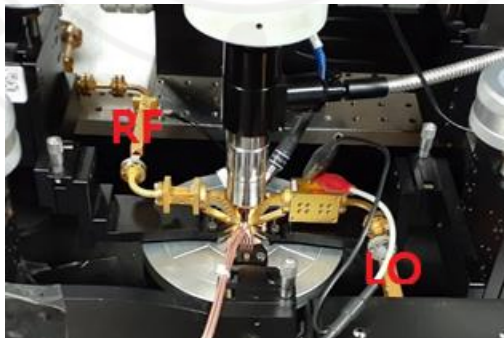


Figure 6.15. Measurement setup for the gain of the mixer-first 280-GHz Rx.

The mixer-first 280-GHz receiver is fabricated on a 130-nm SiGe technology. A photo of the measured chip is shown in Figure 6.14. The chip size of the Rx is  $610 \times 830 \text{ um}^2$ . We measure the gain of the Rx using continuous-wave measurement. The RF signal is generated

from a SAX VDI 3.4. Meanwhile, the LO signal is generated from an SGX VDI 2.8 which is then amplified by using a driving amplifier to generate a larger LO signal for the Rx. The IF signal is measured on the spectrum analyzer Anritsu MS2668C: 9kHz-40GHz. We also measured the connection losses at IF and RF and calibrated these losses from the measured gain. On measurement, the receiver could achieve a peak gain of 15.3 dB, and it is better than 11.2 dB in 259.7-299.2 GHz as shown in Figure 6.16. As can be seen, the simulated gain is more optimistic, especially at high frequencies. Figure 6.17 compared the measured and simulated NF and  $S_{22}$  of the receiver. The measured  $S_{22}$  is fitted well with the simulation results. Meanwhile, the NF was seen to be slightly better on measurement, which is recorded to be 23.2-26.6 in the measured range.

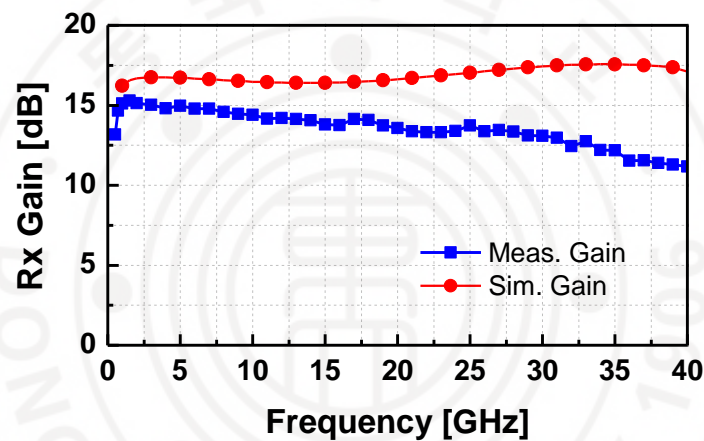


Figure 6.16. Measured and simulated gain of the 280-GHz Rx.

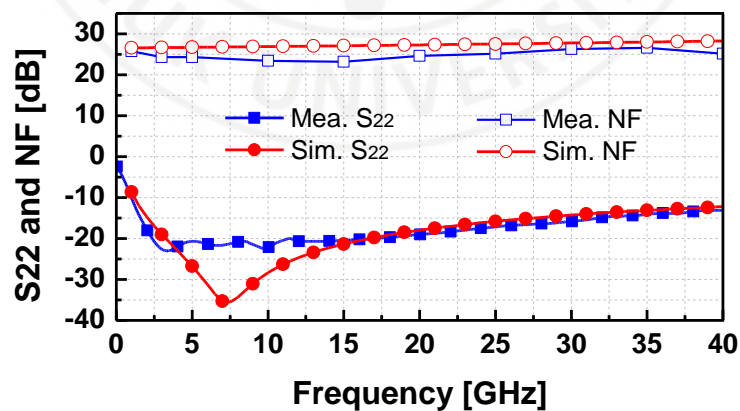


Figure 6.17. Measured NF and  $S_{22}$  of the 280-GHz receiver.

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#### APPENDIX A

From section 6.1 we can write the equations for the condition of conjugate impedance matching at both sides as

$$\left\{ \begin{array}{l} y_S^* = y_{11} - \frac{y_{12}y_{21}}{y_{22} + y_L} \end{array} \right. \quad (A1)$$

$$\left\{ \begin{array}{l} y_L^* = y_{22} - \frac{y_{12}y_{21}}{y_{11} + y_S} \end{array} \right. \quad (A2)$$

$$\Rightarrow \left\{ \begin{array}{l} y_S = y_{11}^* - \frac{y_{12}^*y_{21}^*}{y_{22}^* + y_L^*} \end{array} \right. \quad (A3)$$

$$\left\{ \begin{array}{l} y_L^* = y_{22} - \frac{y_{12}y_{21}}{y_{11} + y_S} \end{array} \right. \quad (A4)$$

Using (A4) in (A3), we get

$$y_S = y_{11}^* - \frac{y_{12}^*y_{21}^*}{y_{22}^* + y_{22} - \frac{y_{12}y_{21}}{y_{11} + y_S}}$$

$$\Rightarrow G_{22}y_S^2 + j\{2G_{22}B_{11} - \text{Im}[y_{12}y_{21}]\}y_S + \text{Re}[y_{11}^*y_{12}y_{21}] - G_{22}|y_{11}|^2 = 0 \quad (A5)$$

If  $G_{22}=0$  then

$$y_S = \frac{j\text{Re}[y_{11}^*y_{12}y_{21}]}{\text{Im}[y_{12}y_{21}]} \quad (A6)$$

If  $G_{22} \neq 0$

$$y_s = \frac{-j[2G_{22}B_{11} - \text{Im}(y_{12}y_{21})] \pm \sqrt{\Delta}}{2G_{22}} \quad (\text{A7})$$

where:

$$\begin{aligned} \Delta &= \{j[2G_{22}B_{11} - \text{Im}(y_{12}y_{21})]\}^2 - 4G_{22}[\text{Re}(y_{11}^*y_{12}y_{21}) - G_{22}|y_{11}|^2] \\ \Delta &= -[4G_{22}^2B_{11}^2 + [\text{Im}(y_{12}y_{21})]^2 - 4G_{22}B_{11}\text{Im}(y_{12}y_{21})] \\ &\quad - 4G_{22}\left[\text{Re}\left\{\begin{pmatrix} G_{11} & - \\ jB_{11} & \end{pmatrix} \begin{bmatrix} \text{Re}(y_{12}y_{21}) \\ j\text{Im}(y_{12}y_{21}) \end{bmatrix}\right\} - G_{22}|y_{11}|^2\right] \\ \Delta &= 4G_{11}^2G_{22}^2 - [\text{Im}(y_{12}y_{21})]^2 - 4G_{11}G_{22}\text{Re}(y_{12}y_{21}) \end{aligned} \quad (\text{A8})$$

Using the formula of  $K$  section 2.1, we obtain

$$\Delta = |y_{12}y_{21}|^2 (K^2 - 1) \quad (\text{A9})$$

Replacing (A9) into (A7) yields

$$y_s = \frac{j[\text{Im}(y_{12}y_{21}) - 2G_{22}B_{11}] \pm |y_{12}y_{21}|\sqrt{K^2 - 1}}{2G_{22}} \quad (\text{A10})$$

Replacing  $y_s$  in (A4) to (A4), we get the formula of  $y_L$ :

if  $|K| \geq 1$

$$y_L = \frac{j[\text{Im}(y_{12}y_{21}) - 2G_{11}B_{22}] \pm |y_{12}y_{21}|\sqrt{K^2 - 1}}{2G_{11}} \quad (\text{A11a})$$

if  $|K| < 1$

$$y_L = \frac{j[\text{Im}(y_{12}y_{21}) - 2G_{11}B_{22}] \mp |y_{12}y_{21}|\sqrt{K^2 - 1}}{2G_{11}} \quad (\text{A11b})$$

Considering the solution of non-negative  $G_s$  and  $G_L$ , and when  $|K| \geq 1$ , (A10) (A11a) becomes the solution in section 6.1.