Thesis for the Degree of Master of Engineering

Design of 8 bit Current Steering RF DAC for Direct Digital Synthesis in CMOS Technology

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by

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ABSTRACT

This thesis proposes an 8 bit current steering digital-to-analog circuits in RF frequency band required for direct digital synthesizer. Unlike the existing superheterodyne transmitter method, the direct digital synthesis method has the convenience of replacing the complex synthesis and filter method with an RF DAC. Accordingly, the RF DAC has a high Spurious-Free Dynamic Range (SFDR) performance is required. There are various types of architectures in current steering DAC, but among them, the time interleaving structure and basic structure DAC is designed. Three versions of 8 bit DAC are designed, 8 GS/s time interleaved DAC and 16 GS/s basic DAC are designed in Samsung 28 nm technology, and 12 GS/s basic DAC is designed in TSMC 40 nm technology. In the implemented single channel 12 GS/s DAC shows, 8 bit Effective Number of Bit (ENOB), 69.4 dB Signal-to-Noise Ratio (SNR), and 75.8 dBc SFDR at Nyquist frequency (6 GHz) through post layout simulations.

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Chapter 1 Introduction

With the development of CMOS technology, the strength of digital integrated circuits is increasingly being highlighted. The density of circuits is increasing, the speed of circuits is increasing, and the power consumption of circuits is decreasing by the scaling of supply voltage and CMOS channel length scaling. Since the threshold voltage of MOS is not scaled at the same rate as the degree to which the supply voltage is scaled, the advancement of the CMOS technology does not directly lead to performance improvement in Analog and RF circuits. On the other hand, the advancement of the CMOS technology lead to direct performance improvement in Digital circuits because capacitance and signal swing are reduced due to channel length scaling and supply voltage scaling. Therefore, unlike the transceiver of the analog (RF) front end and the data converter of the baseband, the performance of the DSP, which is mainly in the digital domain, is improved. Accordingly, the performance of ADCs and DACs acting as an interface system between the back end DSP and the analog (RF) front end is becoming more and more important. Analog-to-Digital Converter (ADC) is a system that converts signals in the real analog world into digital signals and is used for signal reception. Conversely, Digital-to-Analog Converter (DAC) is a system that converts digital signals into analog signals and is used for signal transmission. In this thesis, DAC is mainly dealt with, and in addition to that, RF DAC is the main topic. In order to directly design RF DAC, a digital

circuit configuration capable of delivering data with a high sampling rate is essential, and an analog circuit configuration capable of extracting analog output from this data is also essential. Therefore, in the case of mixed signal circuits such as ADC and DAC, knowledge of digital and analog circuits and knowledge of RF and signal processing are also very important. Apart from the theoretical parts, it explains the problems and solutions that have actually been experienced in designing RF DAC.

Chapter 2: Before the main topic of this thesis, a description of the characteristics of DAC is included. This chapter explains basic operation information of DAC and information on static / dynamic performance of DAC. There is a description of the structure and type of DAC, and in this thesis, current steering DAC with segmented structure is used. Based on the above information, chapters 5 and 6 suggest solutions to problems in actual DAC design and application.

Chapter 3: This chapter contains a description of the main topic, Current Steering DAC (CS DAC). The basic operations and performances of the DAC presented in Chapter 2 are explained by applying it to the CS DAC. It also includes intuitive descriptions of modeling and analysis of the CS DAC. The main content of this chapter is an explanation of the parts that require some consideration in the actual design process.

Chapter 4: This chapter contains a description of the memory that supplies the digital data corresponding to the input of the DAC and the SPI interface that enables calibration. A DAC is a system of a parallel digital input to serial analog output type,

as opposed to an ADC of a serial analog input to parallel digital output type. The DAC in the actual transceiver receives the input through the DSP, so it is not designed in the same area, whereas if an independent DAC system is designed, a memory that can act as its own digital input system is required. Since the operation of memory in real world designs directly affects the operation of DACs, the design of memory is essential and critical.

Chapter 5: This chapter includes a description of the basic operating principle of the Time Interleaved DAC, as well as its disadvantages and advantages. In addition, there is a description of the actual implementation process and the entire block diagram and configuration circuits of Time Interleaved DAC. It is designed in a different way from the existing papers, and there is a performance improvement accordingly. The explanation of the newly applied method is interpreted based on the information in chapter 3 and improvements are suggested. Finally, the conclusion and the possibility and development direction for Time Interleaved DAC are presented.

Chapter 6: This chapter includes descriptions of the basic operating principles and types of current steering DACs, as well as their advantages and disadvantages. Additional explanation is given by applying the information of chapter 2 to the actual current steering DAC. There is an implementation method for each current steering DAC, a block diagram, and a description of the configuration circuits. This thesis approaches from a different point of view from the existing papers and explains the

theory and logic. Conclusion and current steering DAC development direction and supplementary points are presented.

Chapter 7: In the last of the thesis, there is a summary of the DAC described so far and the improvements compared to the existing ones are explained. This chapter presents the possibility and application for RF DAC.

Chapter 2 Digital-to-Analog Converter

2.1 Introduction of DAC

DAC is a system that acts as an interface between the digital world and the analog world. A DAC with digital input to analog output characteristics is used in the transmitter structure, and DAC used from the existing complex superheterodyne structure to the latest Direct Digital Synthesizer (DDS) is an essential system. In the case of RF DAC used in DDS, it enables a very simple method of transmitting a signal through only a filter and a PA, bypassing the conventional upconversion method. Therefor, the performance of the RF DAC is becoming more and more important now, and research on the RF DAC is being actively conducted accordingly. The implementation method mainly used for RF DAC is Current Steering (CS) DAC, and although the operation method and configuration circuits of CS DAC look simple, the actual design is very difficult. Before explaining the CS DAC, which is the main subject of this thesis, in this chapter, the basic characteristics of the DAC are explained.

2.1.1 Basic Principle of DAC

DAC is an abbreviation for digital input to analog output converter, so a digital input is required for DAC. Also, since it is parallel to serial conversion, if it is an N-bit DAC, at least N parallel data coming at the same timing is required. These digital data are generally generated by DSP or memory at an appropriate sampling rate and

then fed into the DAC. Accordingly, at the output of the DAC, an analog value suitable for digital data can be maintained for a time of 1 / sampling rate (Fs). Theoretically, the N-bit DAC has 2^N states within the output swing range, and it can generate sinusoidal outputs of various frequencies that fit the data up to the Nyquist frequency of the maximum sampling rate. Figure 2.1-1 shows the sinusoidal signal of Fs / 16 at the output of the DAC.

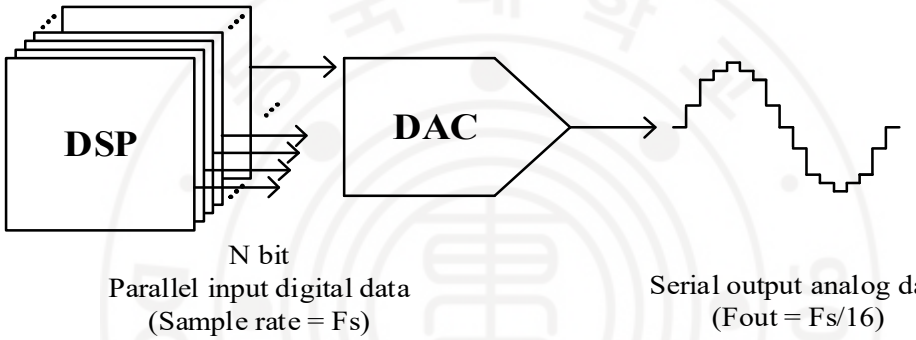

Figure 2.1-1. Input-to-Output Transformation of N-bit DAC

2.1.2 Basic Principle of Current Steering DAC

An ideal DAC has an ideal value for each digital code. The value is divided into voltage, current, and electric charge according to the implementation options of DAC. In the case of CS DAC, it can be seen that the analog value is current. If it is an N-bit CS DAC, it has a total of 2^N states. At this time, the difference between the analog values of adjacent digital codes becomes full scale current $/2^N - 1$, and this value is called 1 LSB. Through this, unit current / voltage / electric charge can be set according to the desired full swing range. Figure 2.1-2 shows the transfer function of 3-bit Ideal DAC and CS DAC. When looking at the output of the CS DAC in

terms of voltage, it can be seen that it shows the opposite tendency to the transfer function of ideal DAC.

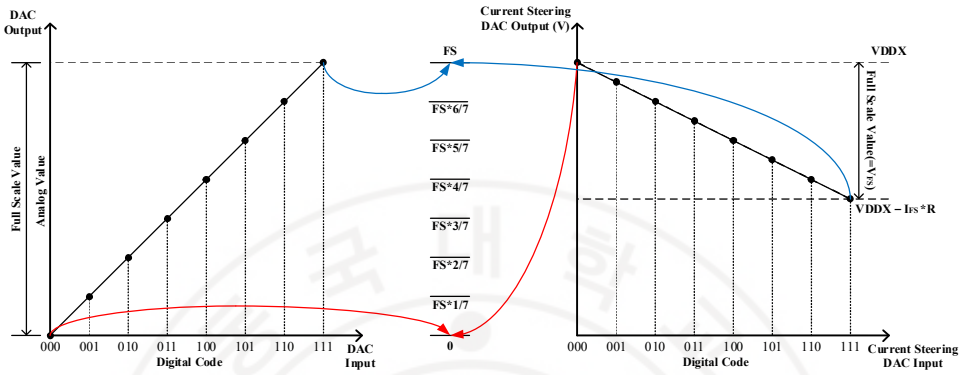

Figure 2.1-2. 3 bit Ideal DAC & Current Steering DAC Transfer Function

2.2 Static Performance of DAC

Static performance refers to the performance of the DAC in the low frequency band. As the frequency band of DAC gradually increased, dynamic performance become important. However, it is important to note that it is static performance that greatly affects the value of the actual DAC analog output. The analog output value at this time means the settling value. Unlike dynamic performance, it can be checked in the time domain.

2.2.1 Offset Error

Offset error means the difference between the ideal value and the actual value when the digital code is 0. Figure 2.2-1 shows the offset error transfer function of the 3 bit DAC. In this case, the actual value is a value that assumes only the offset error in DAC. The full scale value is maintained, and it can be seen that the value is

constantly changed by the offset. A negative offset is also possible. If it is an actual current steering DAC, the value of the output voltage when the digital code is 0 would have been less than VDDX. In terms of output current, it is a positive effect.

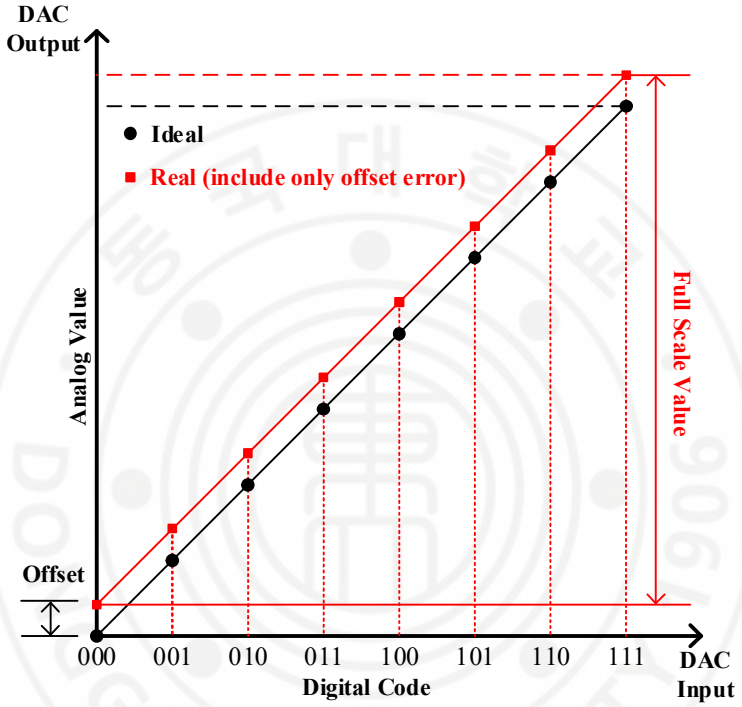

Figure 2.2-1 Offset Error of a 3 bit DAC Transfer Function

2.2.2 Gain Error

Gain error means the difference between the slope of the linear transfer curve between the ideal transfer function and the actual transfer function. At this time, the linear transfer curve is a straight line connecting the analog values when the digital code is the minimum and maximum. Therefore, if there is no offset error, the gain error will be the ratio of the analog values of the maximum digital code. Figure 2.2-

2 shows the gain error transfer function of a 3 bit DAC. In this case, the actual value is a value that assumes only the gain error in DAC. If this situation is applied to the current steering DAC, it can be seen that the larger the slope, the larger 1 LSB current than the ideal 1 LSB current.

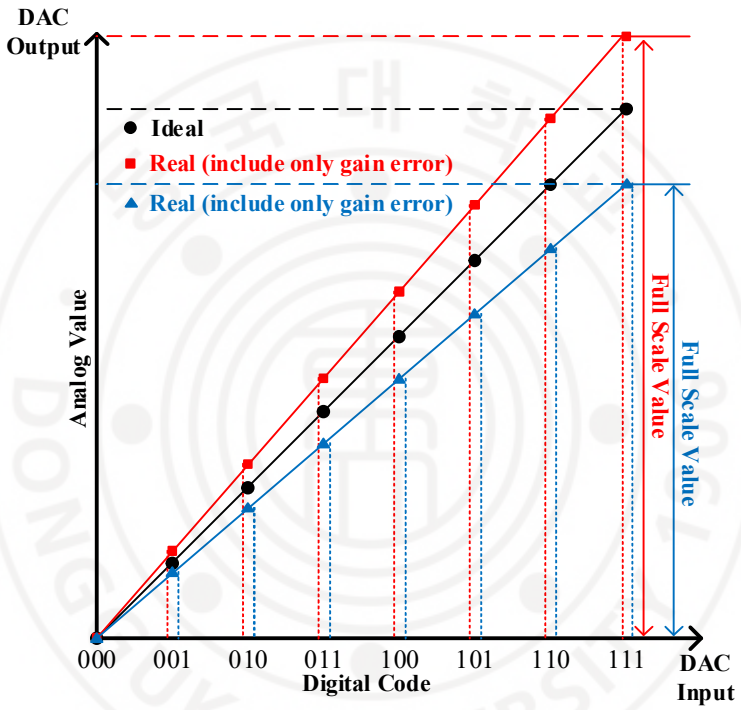

Figure 2.2-2 Gain Error of a 3 bit DAC Transfer Function

2.2.3. Nonlinearity Error

So far, there have been only errors that do not affect the linearity of the DAC, but there are actually many sources that cause nonlinearity. Since the nonlinearity source differs according to the implementation option of the DAC, this will be explained in chapter 5. Figure 2.2-3 shows the nonlinearity error transfer function of

a 3 bit DAC. The source that induces nonlinearity in the CS DAC is the current source, and it is largely divided into systematic error and random error. In summary, it means that the amount of current in each current sources is not constant.

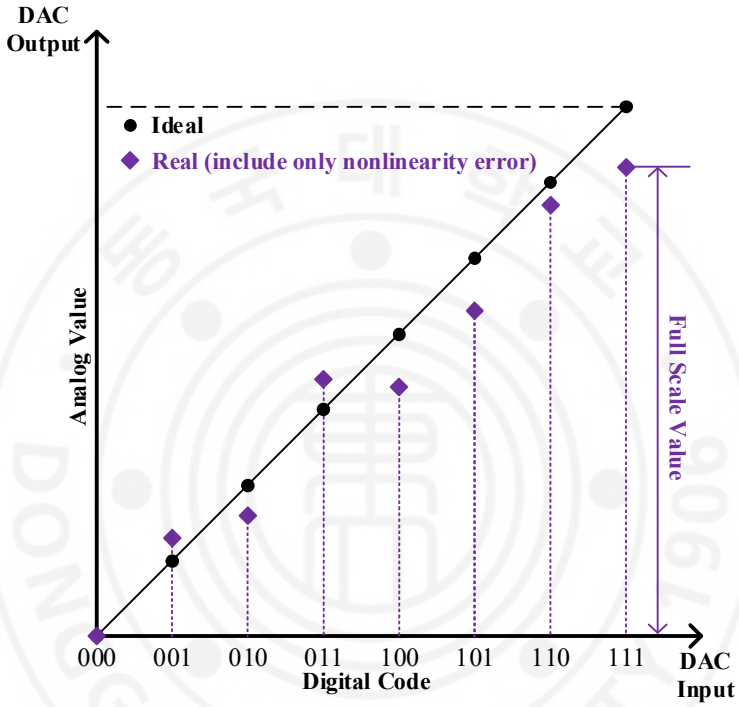

Figure 2.2-3 Nonlinearity Error of a 3 bit DAC Transfer Function

2.2.4. DNL & INL

DNL is an abbreviation for Differential Nonlinearity, and INL is an abbreviation for Integral Nonlinearity. DNL error is the difference between the analog values of adjacent digital codes minus the reference value. In this case, the reference value is 1 LSB.

$$\text{DNL(n) [LSB]} = (Code_n[LSB] - Code_{n-1}[LSB]) - 1[LSB] \qquad (2.2.4.1)$$

INL error is the sum of DNL errors from digital code 0 to the current code.

$$\text{INL(n) [LSB]} = \sum_{k=0}^{i} DNL(k)[LSB] \quad (2.2.4.2)$$

Before finding these errors, it is necessary to remove the offset error and gain error from the actual transfer function. Figure 2.2-4 shows the process of offset / gain error compensation of 3 bit DAC transfer function. First, the offset error is removed from the actual transfer function, and then scaling is performed as much as the gain error. Figure 2.2-5 shows the result of offset / gain error compensation of 3 bit DAC transfer function. As explained earlier, the difference between the analog values of adjacent codes is DNL(n) + 1LSB. Figure 2.2-6 shows the DNL and INL values obtained after normalizing the real transfer function to the ideal transfer function in Figure 2.2-5.

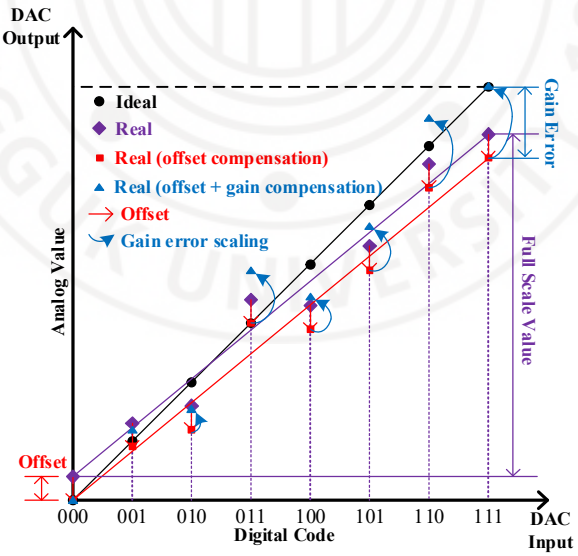

Figure 2.2-4 Offset & Gain Error Compensation Process of a 3 bit DAC Transfer Function

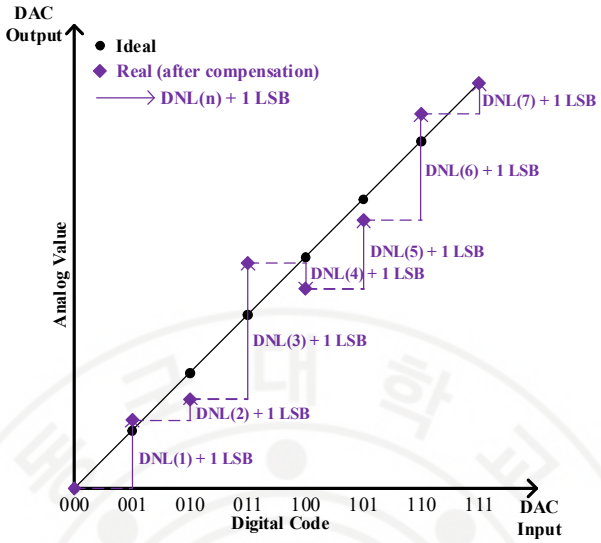

Figure 2.2-5 After Offset & Gain Error Compensation of a 3 bit DAC Transfer Function

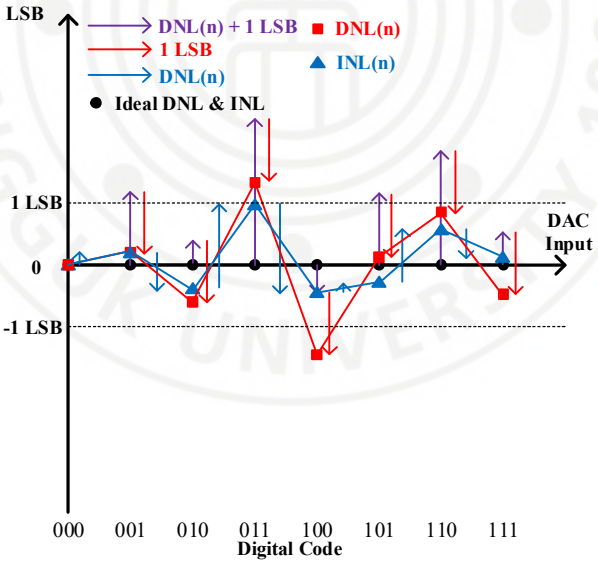

Figure 2.2-6 DNL & INL of a 3 bit DAC Transfer Function

2.3 Dynamic Performance of DAC

2.3.1. SFDR

Among the dynamic performance of DAC, the most important is SFDR. SFDR measures the relative power of the desired signal to the power of the highest spur component generated within the targeted bandwidth.

$$\text{SFDR [dBc]} = 10\log_{10}\left(\frac{P_{signal}}{Highest\ Spur\ Power}\right) \quad (2.3.1)$$

2.3.2. SNR

Signal-to-noise ratio is defined as the ratio of the desired signal power to the integrated noise power, excluding harmonics and DC offset. Typically, the specified noise power includes quantization noise, DNL error, thermal noise, and random jitter.

$$\text{SNR [dB]} = 10\log_{10}\left(\frac{P_{signal}}{N_q+N_{DNL}+N_{Thermal}+N_j}\right) \quad (2.3.2)$$

2.3.3. SNDR & ENOB

Signal-to-Noise-and-Distortion-Ratio (SNDR) measures the ratio of the power of the desired signal to the power of the total noise, including harmonic distortion products.

$$\text{SNDR [dB]} = 10\log_{10}\left(\frac{P_{signal}}{N_q+N_{DNL}+N_{Thermal}+N_j+P_{Distortion}}\right) \quad (2.3.3.1)$$

ENOB is used to represent the effective resolution of the converter including all sources of noise and/or distortion.

$$\text{ENOB [bit]} = \frac{(SNR \ or \ SNDR)[dB] - 1.76}{6.02} \quad (2.3.3.2)$$

2.4 Architectures of DAC

The architecture of the DAC depends on how the elements used are divided. DAC architectures include binary, thermometer, and segmented coded structures.

2.4.1. Binary Coded DAC

Since the input to a DAC is binary digital word, every input bit corresponds to binary weighted element. Binary coded DAC has advantages in area and power consumption because the number of decoding circuits can be minimized. However, there is a disadvantage that it is difficult to match the current source and accordingly the errors of INL and DNL are large. Figure 2.4-1 shows the binary coded DAC alignment.

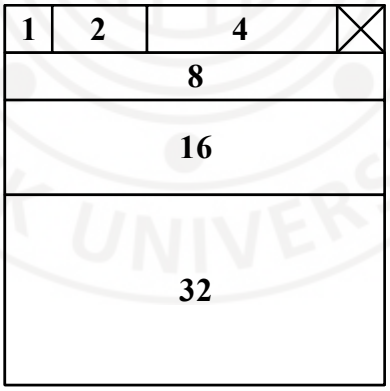

Figure 2.4-1 Binary Coded DAC Alignment

2.4.2. Thermometer Coded DAC

Thermometer coded DAC drives the switch by converting the incoming binary

data into a thermometer code. Therefore, N to 2^N binary to thermometer decoder is required, and it is composed of 2^N-1 unit current. It has the advantage of small INL and DNL errors. There are disadvantages in terms of area and power consumption due to the large number of switches and decoders. Figure 2.4-2 shows the thermometer coded DAC alignment.

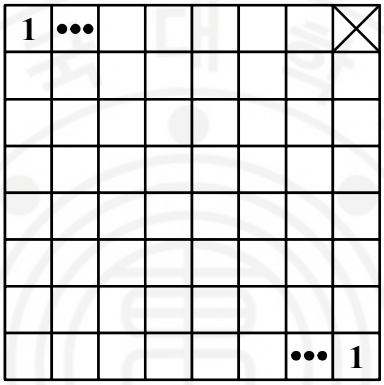

Figure 2.4-2 Thermometer Coded DAC Alignment

2.4.3. Segmented Coded DAC

Because the advantages and disadvantages of the binary structure and the thermometer structure are balanced, it is the most widely used structure among the DAC architectures. Figure 2.4-3 shows the segmented coded DAC alignment.

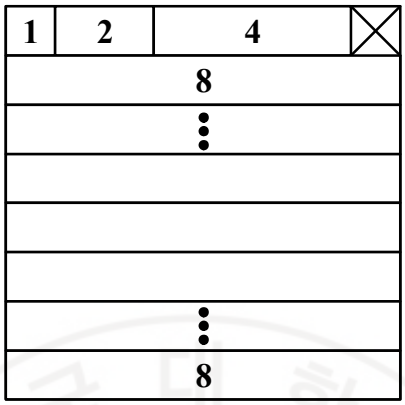

Figure 2.4-3 Segmented Coded DAC Alignment

2.5 Implementations of DAC

Depending on how an element is implemented, there are three basic DAC physical implementations. DAC implementation options include resistor, capacitor, and current.

2.5.1. Resistor DAC

By connecting or disconnecting the resistors, the output voltage is controlled by the input binary bits. The resistor DAC accuracy depends on the matching of the resistors. Speed and linearity are main limits of resistor type DACs due to the nonlinear resistors and the bandwidth and linearity of the OPAMP. Figure 2.5-1 shows the 5 bit binary coded R-2R DAC.

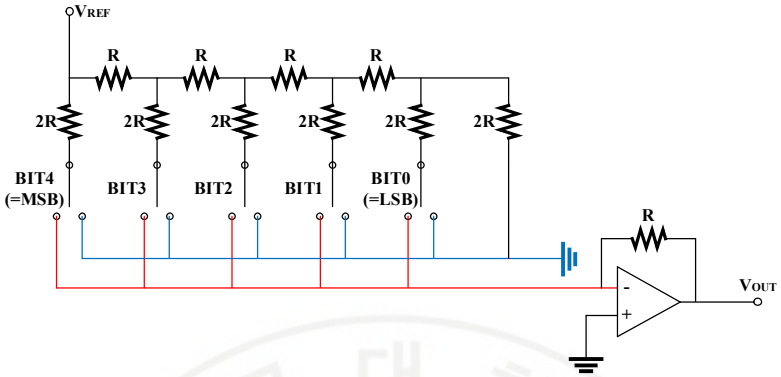

Figure 2.5-1 5 bit Binary Coded R-2R DAC

2.5.2. Capacitor DAC

Based on charge conservation, the output voltage is a fraction of V_{REF} which is set by the input digital code. Similar to the resistor DAC, the capacitor DAC's accuracy depends on the matching of the capacitors [24]. Speed and linearity are also main limits of this capacitor type of DAC. Figure 2.5-2 shows the 5 bit binary coded capacitor DAC.

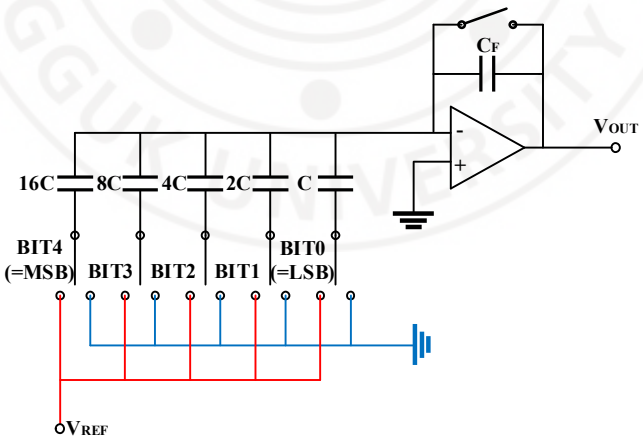

Figure 2.5-2 5 bit Binary Coded Capacitor DAC

2.5.3. Current Steering DAC

With the rapid development of communication systems, such as DDS and novel RF transceivers in new applications, high speed and high resolution DACs are required. The CS DAC is a suitable architecture for such applications, because of its intrinsic high speed and driving capability. The current cell consists of a current source and differential switches, and the current is switched to the positive output node or to the negative output node according to the input digital bit. Also, the CS DAC's accuracy relies on the matching between current sources. Figure 2.5-3 shows the 5 bit binary coded current steering DAC.

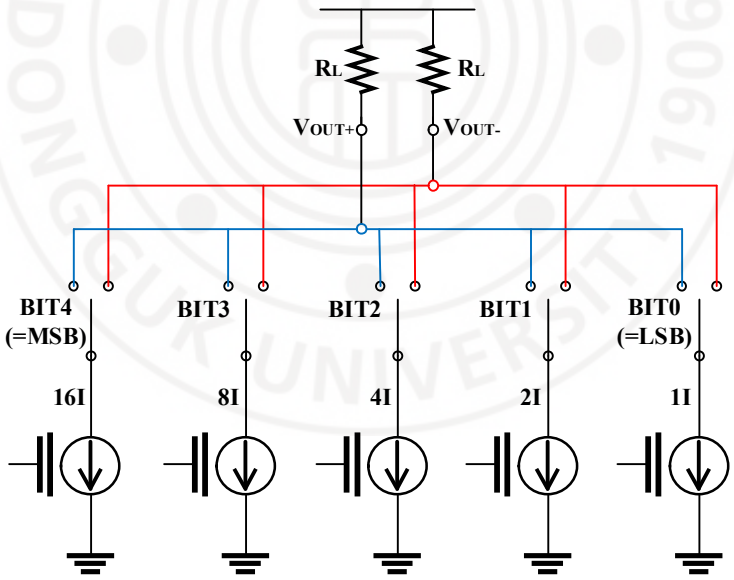

Figure 2.5-3 5 bit Binary Coded Current Steering DAC

Chapter 3 Current Steering Digital-to-Analog Converter

3.1 Introduction of Current Steering DAC

So far, the basic DAC has been described, and in this chapter, there is a description of the CS DAC. CS DAC generally use MOS device as a current source and operate in such a sway that the change in current according to the digital code changes to output voltage. Due to the nature of MOS, the current source of the CS DAC is not stable. This means that the current flowing from the current source changes without being constant, and the drain voltage of the current source has the greatest effect on this in the CS DAC. Therefore, it is important to design it to allow a stable current to flow to some extent even when the drain voltage changes. The parameter that has the greatest influence on this is the length of MOS. Figure 3.1-1 shows the explanation of this.

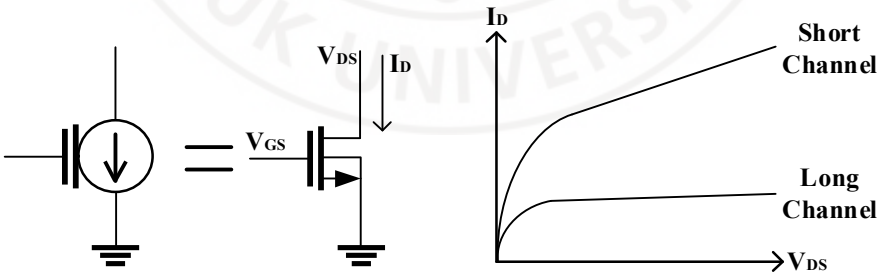

Figure 3.1-1 Simple MOS Current Source Variation according to the Drain Voltage & Channel Length

As can be seen from the figure above, the longer the length of MOS, the smaller

the change in current in accordance with the change in drain voltage. In this case, the MOS is operating in the saturation region. In the actual CS DAC, a cascode device is generally added on top of the current source to allow a more stable current to flow. This is also to prevent the change in source voltage due to the change in drain voltage of the switch from directly affecting the drain voltage of the current source. Although there is a possibility that a short channel device may be used using this, a long channel device is used in this thesis due to problems such as yield and device mismatch.

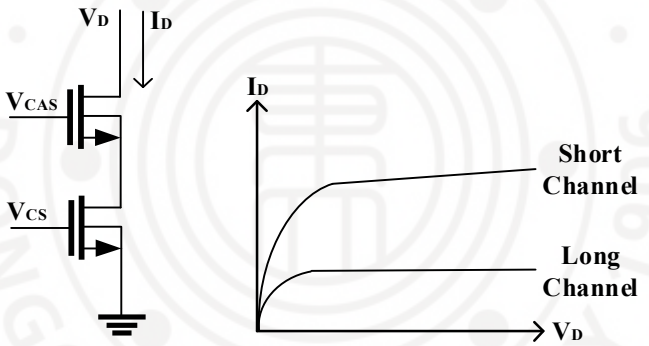

Figure 3.1-2 Simple MOS Cascode Current Source Variation according to the Drain Voltage & Channel Length

CS DAC's analog core cell is a form in which a differential pair switch capable of receiving a digital code is added on the cascode device described above. It is important to see the switch used in this case from the perspective of an analog switch, not a general digital switch. Therefore, the switch must also have the ability to flow as much as the amount of current specified below. Otherwise, it may affect the operating region of CS DAC, which leads to performance degradation. In addition,

the data signal applied to the gate of the switch should be viewed from an analog perspective rather than digital. This is because the quantity of voltage of gate also affects the current quantity of the actual switch device. However, this can be ignored to some extent if the devices operate in the saturation region sufficiently. However, it should be noted that if the data are not stable and there are many fluctuations, the output voltage waveform of CS DAC will also not be stable.

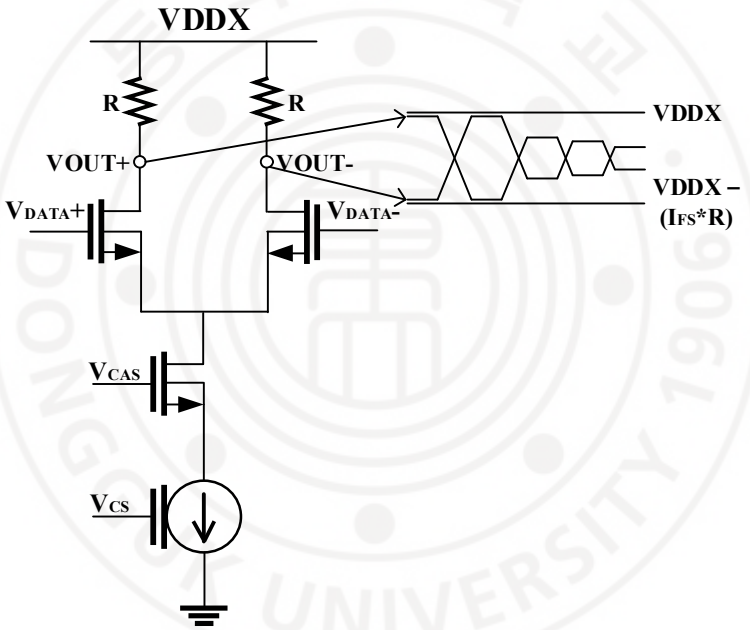

Figure 3.1-3 Simple Current Steering DAC Structure

3.2 Static Nonlinearity of Current Steering DAC

As with MOS used as a current source, there are factors that affect the linearity of CS DAC. Among them, static nonlinearity is first described. Static nonlinearity refers to the nonlinearity occurring in DC (=low frequency), which generally occurs

in a steady state. In other words, it can be said that it is about the nonlinearity of the current quantity. In general, static nonlinearity affects the INL and DNL performance of CS DAC. There are graded error, symmetrical error, random error, and finite output impedance that affect static nonlinearity.

3.2.1. Graded & Symmetrical Error

When classifying, graded error and symmetrical error can be checked first. It can be said that the core of these errors is the difference in the amount of current due to the discrepancy in GNDX. This refers to the problem that the same amount of GNDX is not applied to all current sources due to the voltage drop present in the GNDX line. As a result, the overdrive voltage applied for each current source is different, so there is a difference in current. In fact, voltage drops also exist in the bias line and the current signal line of the current source.

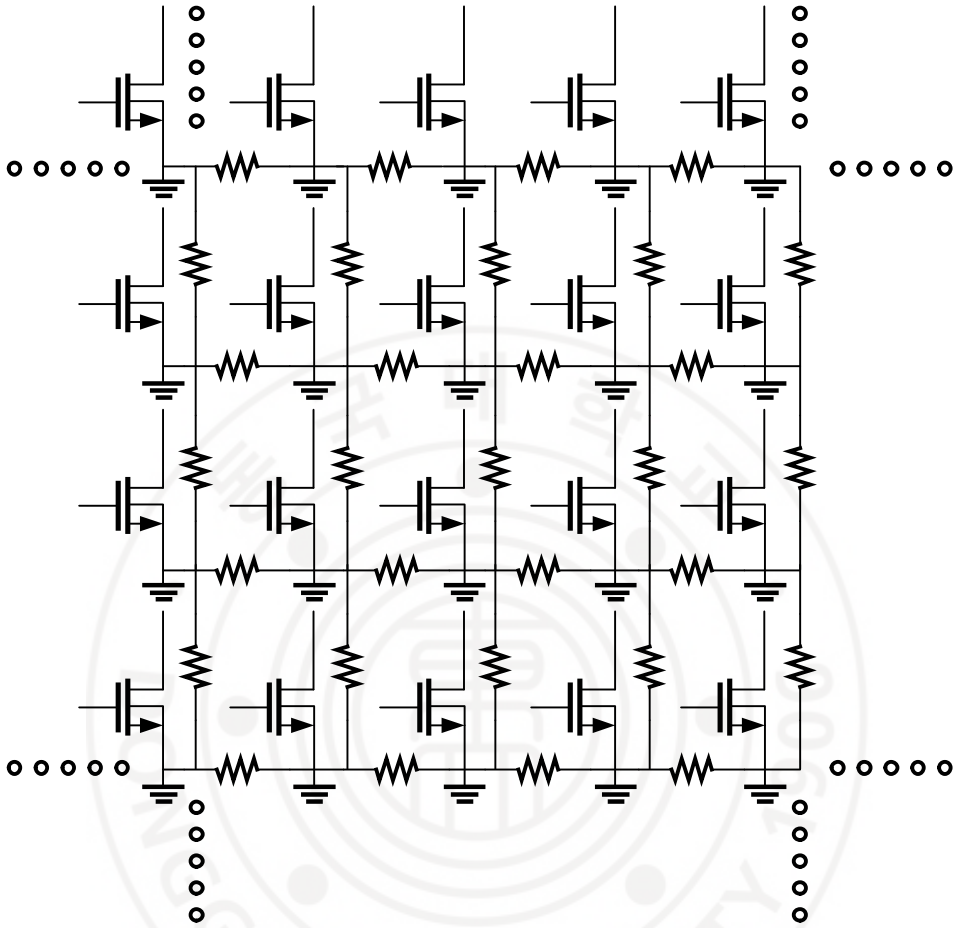

Figure 3.2-1 Voltage Drop Concept over the GNDX Line

Current sources are configured in the form of an array as shown above. Therefore, aspects of these errors vary depending on the location where the GNDX enters and the location where the bias line enters. Design the aspects of the errors as identical as existing papers as possible. The reason is that the switching scheme mentioned in the existing paper is constructed under the assumption of such an error aspect. Therefore, in the actual layout design, the bias and GNDX inputs are placed

in the center of the current source array. Nevertheless, since the exact direction of the current over the GNDX line is not fully known, it can be inferred from the amount of current in each current source. In addition, to reduce these errors, the GNDX line and gate bias line basically use wide lines with less voltage drop. In addition, the degree of these errors is directly affected by the resolution of the CS DAC.

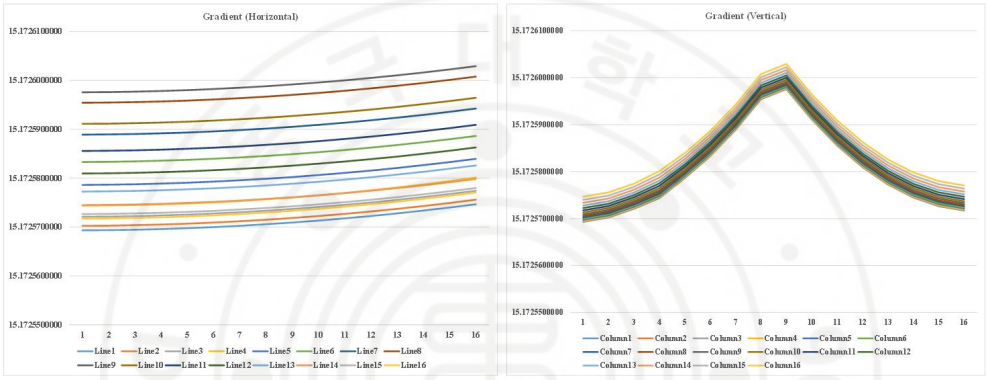

Figure 3.2-2 Graded & Symmetrical Error Profile of the Bias Location at the center at the end of the Current Source Array

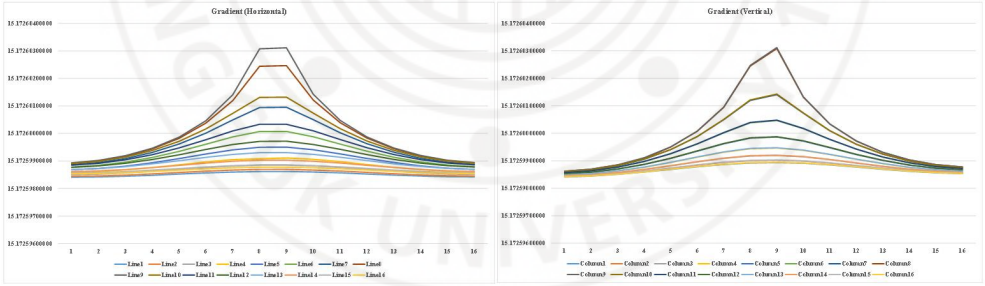

Figure 3.2-3 Graded & Symmetrical Error Profile of the Bias Location at the center of the Current Source Array

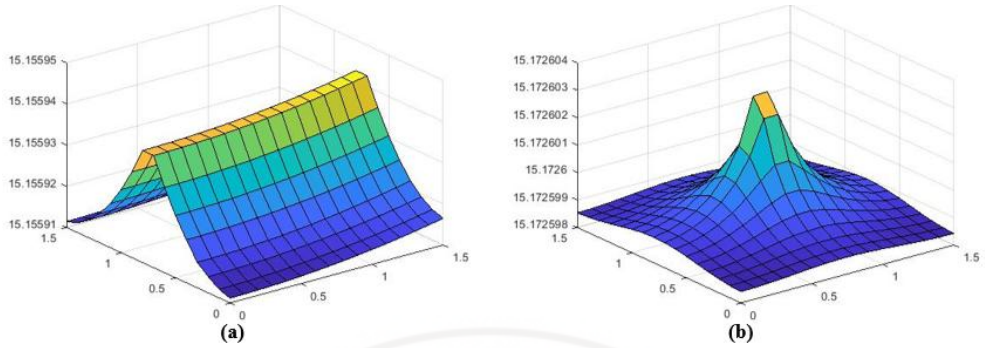

Figure 3.2-4 Graded & Symmetrical Error 3-D Profile (a) Figure 3.2-2 (b) Figure 3.2-3

As can be seen from the figures above, it can be seen that the aspect of graded, symmetrical error varies depending on the bias location. In addition, it can be seen that the pattern of error appears differently depending on the axis direction. Therefore, it is important to set the gate bias and GNDX input positions of the current source array according to the type of switching scheme actually used.

As a result, the switching scheme is used to compensate for this difference in current. Hierarchical switching scheme, Q^2 random walk switching scheme, and Common centroid switching scheme are mainly used.

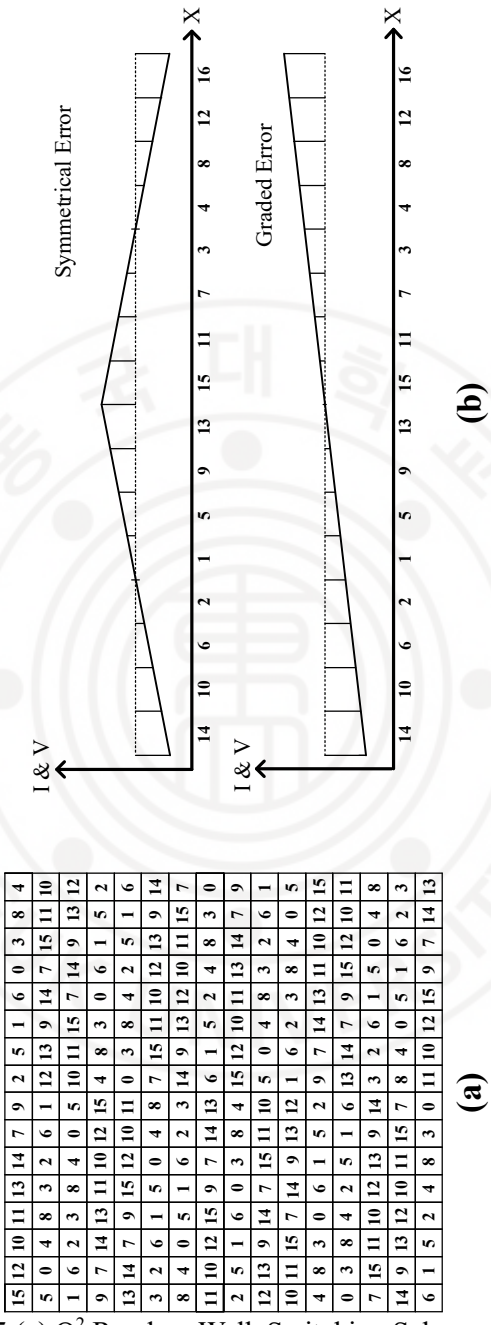

Figure 3.2-5 (a) Q^2 Random Walk Switching Scheme (b) Hierarchical Switching Scheme

3.2.2. Random Error

The following is a description of a random error that affects the nonlinearity of the current. There are mismatch factors that the device itself has due to various factors in the actual CMOS process. Representatively, there are gain factor mismatch and threshold voltage mismatch. As can be seen from the current formula of MOS, the previous two factors are factors that directly affect the current. Due to this device mismatch, there is a formula for the minimum device area to meet the desired yield. This paper designs an 8 bit CS DAC, where to make the DNL spec smaller than 0.5 LSB, the unit current relative standard deviation must be less than 3%, and 1% unit current relative standard deviation is required to achieve 99.7% of the 3 σ yield. The figure below shows the minimum area actually required using the existing formula [3,4].

$$\mathrm{LWmin} = \frac{1}{2}\left(A_{\beta}^{2} + \frac{4A_{VT}^{2}}{(V_{GS}-V_{T})^{2}}\right)/\left(\frac{\sigma_{I}}{I}\right)^{2} \quad (3.2.2)$$

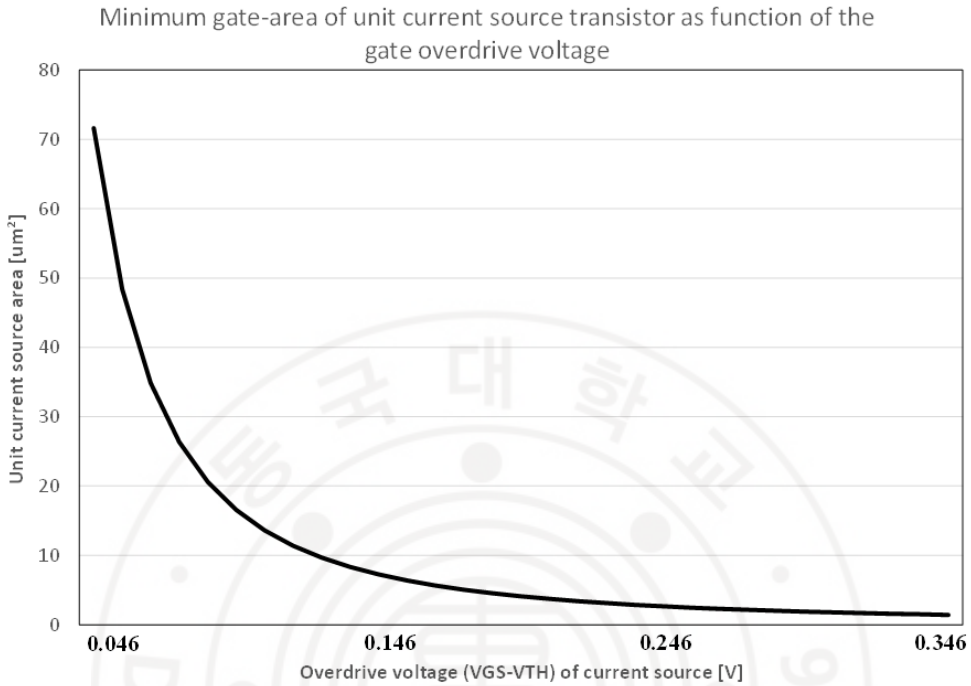

Figure 3.2-6 Minimum Gate-Area of Unit Current Source Transistor as Function of the Gate Overdrive Voltage when 1% Unit Current Relative Standard Deviation

3.2.3. Finite Output Impedance

It is a description of finite output impedance, which is the last of static nonlinearity. This is a nonlinearity that is similar to the graded & symmetrical error described before but has a different perspective. In the case of graded & symmetrical error, if it is caused by the bias line voltage drop or the GNDX line voltage drop of the current source, the finite output impedance is caused by the change in the drain voltage of the current source. In this case, it is the output voltage of the CS DAC that affects the drain voltage. The output voltage of the CS DAC has 2^N steady state voltages from zero to full scale depending on the digital code. This means that the drain

voltage of the cascode and current source also has the same number of states as the state of the output voltage. Therefore, this means that the current source is not constant as a result. Therefore, in designing an actual CS DAC, it is important to satisfy the high output impedance of the current source, which has little change in current even with a change in drain voltage. A current source and a cascode device with a sufficiently long length that satisfy the saturation region can allow a sufficiently stable current to flow. If there is any other way, it is a way to reduce the full scale current of CS DAC. This is because the swing of the output voltage of the CS DAC is reduced, and the swing of the devices below is also reduced. In the case of finite output impedance, it also affects dynamic nonlinearity.

The figure below contains a rough description of the finite output impedance. It shows the situation when it is a single core rather than the entire CS DAC, and it is said in advance that the variation of the drain voltage in the actual CS DAC is not that large. In addition, this core cell is an example of a long channel current source device, and in the case of a short channel current source device, it can be expected that there will be a larger current change. In addition, in the case of A, it is a situation when the operating range of the current source is saturation, and in the case of B, it is a situation when the operating range of the current source is triode. As can be seen here, the current of the current source changes significantly if it is not a saturation operation. In actual CS DAC, there are several such cores and they work in combination.

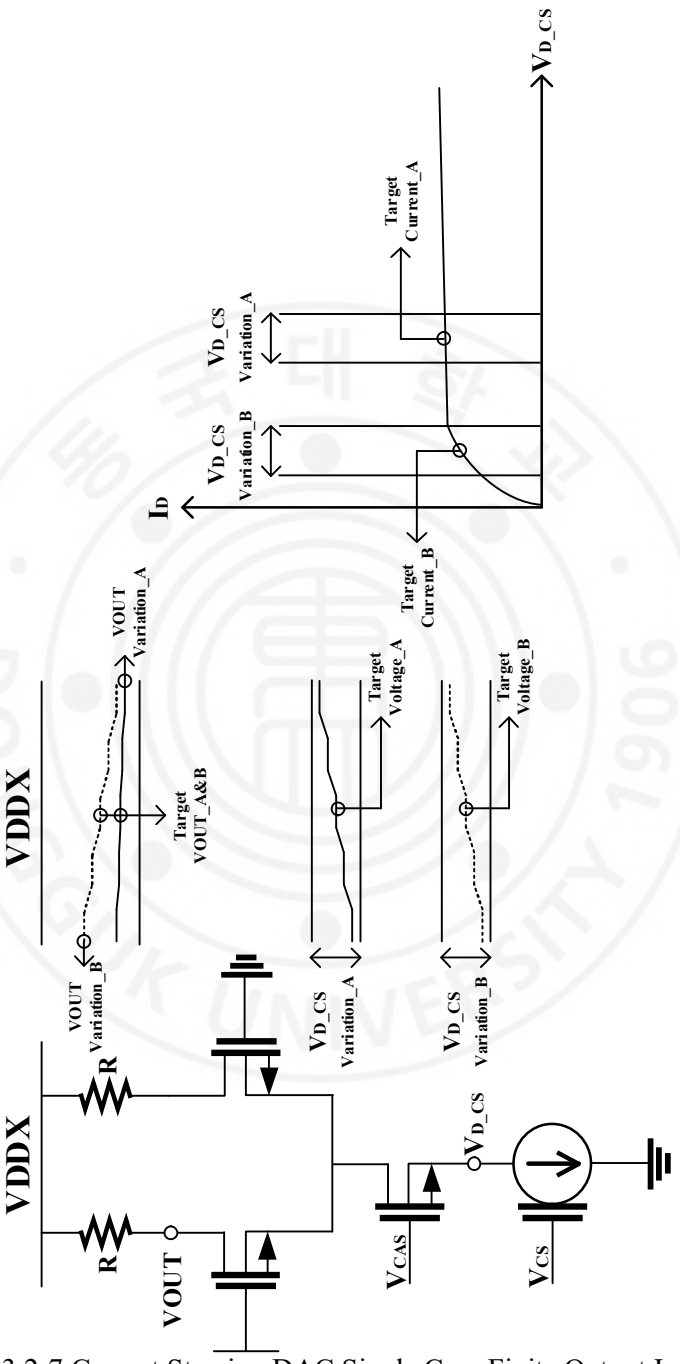

Figure 3.2-7 Current Steering DAC Single Core Finite Output Impedance

3.3 Dynamic Nonlinearity of Current Steering DAC

It contains a description of the dynamic nonlinearity of CS DAC. Dynamic nonlinearity refers to the nonlinearity occurring in high frequency, usually in a transient state. In other words, it can be said that it is about nonlinearity relate to the switching situation. In high frequency, since capacitance acts on the operation of CS DAC, a nonlinearity characteristic is created in the transient situation, which is a switching situation. In general, dynamic nonlinearity affects SFDR performance of CS DAC. Typical examples include glitch, settling time, simultaneously turn off switch, imperfect synchronization, and finite output impedance.

3.3.1. Simultaneously Turn Off Switch

First, a description of a situation in which a differential switch is turned off at the same time is provided. In theory, the switch is turned on when a gate voltage greater than or equal to the turn on voltage (=switch source node voltage + switch threshold voltage) is applied, and turned off when the gate voltage of the switch is less than the turn on voltage. This is a situation when subthreshold operation is not included. In CS DAC, the output voltage and switch data of CS DAC determine this switch turn on point interval. The reason why the switch is turned off at the same time has a bad effect on the CS DAC is that it takes additional time to charge the switch source node voltage after it is discharged. Therefore, in general, when designing CS DAC, the data of the switch is high crossing point (when NMOS current source) data. Therefore, a high crossing point switch driver is generally used

for all stages of the switch. However, even when the switch is turned on at the same time, the source node voltage of the switch changes. In this situation, a differential switch operates in the common mode section, and current distribution occurs. Further explanation of this will be given in Chapter 6. The figure below shows a situation in which the differential switch is turned off at the same time.

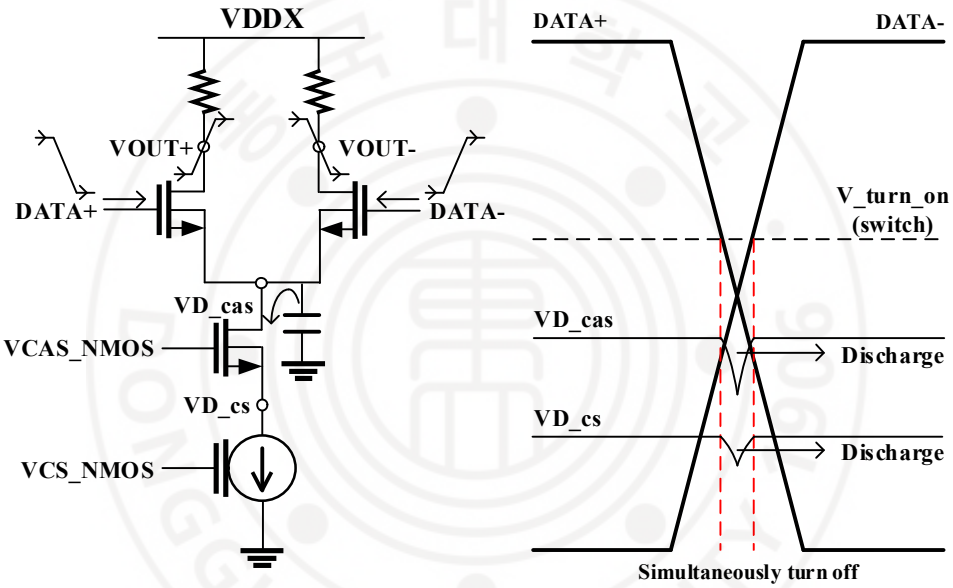

Figure 3.3-1 Simultaneously Turn Off Switch Concept

3.3.2. Imperfect Synchronization

The following is a description of imperfect synchronization. There are several switches that receive data in the CS DAC. Therefore, it can be said that synchronization between data entering the switch is important. If sync doe not fit and the switching interval of the data does not occur at once, it will take additional time for the output voltage to appear according to the digital code, and there is a

possibility that it will not appear in one sampling rate. Therefore, in conjunction with the previous problem, synchronization is achieved by adding a switch driver (Latch or FF) to the previous stage of the switch. In addition, for more accurate synchronization, the current source array method is more advantageous than the row column decoder method. In addition, the parameter of the switch, which is the load of the switch driver, also affects. If the parameters of each switch are different, there is a slight difference in the actual data, but if the difference in the parameters between the switches is not too large, it is negligible.

3.3.3. Glitch & Settling Time

Finally, it is a description of glitch and settling time. It can be said that glitch and settling time are the biggest influences of high frequency's capacitance. In this case, the capacitance includes both the capacitance of the device itself and the parasitic capacitance, and is additionally affected by the change in capacitance caused by the drain source voltage of the switch. In addition, these problems are difficult to control because there is no clear and effective method of improvement after the parameter of the device has already been determined. In general, if the capacitance is large, the glitch and the settling time is large. In addition, even if the amount of current being driven is large, the glitch and settling time will be large. If these two factors are large, in severe cases, a glitch value of a current generated by switching is too large, and thus it takes a long time to return to a previous target current, and thus a current other than an actual desired current may flow. Therefore,

it is recommended that the parameters of the switch and the cascode device be as small as possible, but there is a limit to this method. In addition, reducing the full scale current is one way to reduce the switching capacitance by reducing the change in the source drain voltage of the switch. Since these nonlinearities cannot be fully compensated, they should be designed with trade off in mind.

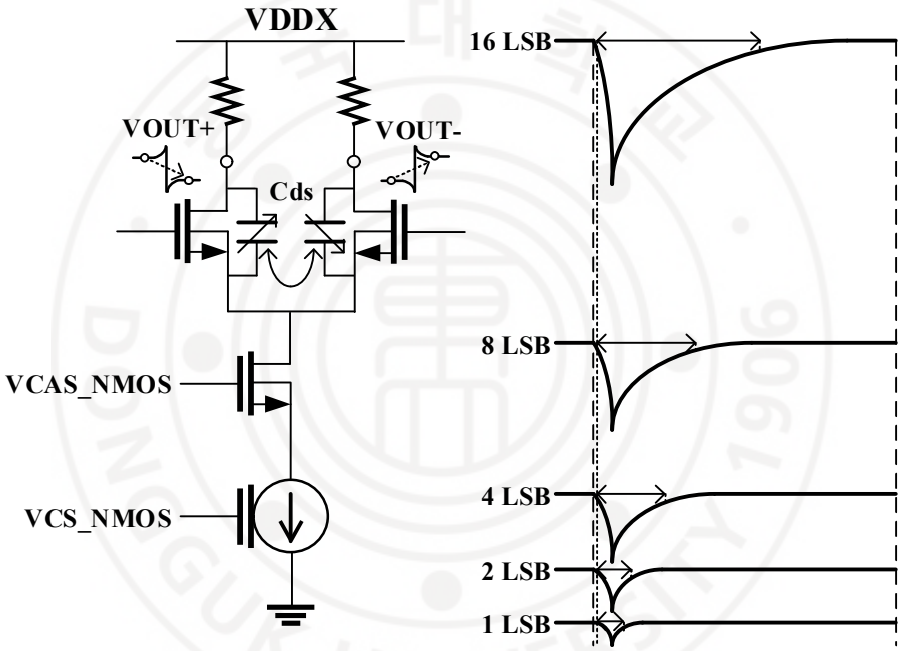

Figure 3.3-2 Glitch and Settling Time Concept

Chapter 4 Concept of Memory in DAC

4.1 Concept of Memory in DAC

The role of memory in an independent DAC system is very important. In order to measure the actual DAC, all digital data must be able to be delivered according to

the target sampling rate. In addition, unlike N bit ADC, which is 1 input to N output, DAC has a form of N input to 1 output. Therefore, all data must enter parallel at the same time, but this can be said to be very difficult due to the constraints of PAD and Chip size and the input that increases in multiple depending on the degree of interleaving of the data. Therefore, memory that can covert a single input into parallel output is an essential system. This means that if the memory does not work properly, the DAC cannot measure itself. It can be said that the role of memory in the DAC system is important.

4.1.1. Target of Memory in DAC

The DAC resolution in this paper is 8 bit. If data interleaving is not required in this DAC, the required memory specification is 1 serial input to 8 parallel output. At this time, 8 parallel output refers to the aligned data of the same time zone. What memory needs to have in order to create such an output is the ability to distribute serial input according to regions and to keep data in each region repeatedly after being distributed. Next, the number of 1 parallel output bit of memory should be more than enough to measure the INL and DNL of the DAC. For an 8 bit DAC, the minimum number of bit in the 1 parallel output of memory will be 256 bit. Until now, it is a memory target in situations where data interleaving is not used, and this situation is rarely used in RF DAC. This is because it is difficult to convert digital data in a high frequency band to parallel output without omission, and it is affected by the presence or absence of measurement equipment that can give such data.

Therefore, data interleaving is generally used to reduce the burden by lowering the sampling input data rate received from the memory. For example, 2 to 1 interleaving in 8 bit DAC, the required memory specification is 1 serial input to 16 parallel output. In this case, the sampling input data rate of the memory becomes half of the DAC sampling rate. However, the disadvantages of this method include difficulty in designing control logic due to the increase in parallel output and an increase in layout size.

It is a description of the target of the memory actually designed in this thesis. First of all, in the case of Time Interleaved current steering DAC designed by Samsung 28 nm process, 2 to 1 data interleaving and 2 to 1 interleaving using an analog multiplexer are performed, and 2 memories are required because there are 2 sub-DACs. A memory has a specification of 1 serial input to 16 parallel output, and the number of bit in 1 parallel output is 128 bit. Since two memory parallel outputs are upconverted to data corresponding to the sampling rate of the DAC through 2 to 1 data interleaving, it satisfies 256 bit, the minimum number of bit in the 8 bit DAC memory. Next, in the case of the basic current steering DAC designed in the Samsung 28 nm process and TSMC 40 nm process, 4 to 1 data interleaving is performed, and 1 memory is required because there is only 1 DAC. At this time, the memory has a specification of 1 serial input to 32 parallel output, and the number of bit in 1 parallel output is 128 bit. Since four memory parallel outputs are upconverted to data that meets the sampling rate of DAC through 4 to 1 data interleaving, 512 bit of data can

be delivered.

4.1.2. Memory Implementation in DAC

It is about the design method of the memory used in the actually designed DAC. It contains only the contents of the memory used in the DAC designed in the TSMC 40 nm. The TSMC 40 nm DAC has a sampling rate specification of 12 GS/s and uses 4 to 1 data interleaving. Therefore, the input data sampling rate of the memory is 3 GS/s, and it has a total of 32 parallel outputs. In this case, each parallel output consists of 128 bit register. If memory is largely classified, it can be divided into a data part, a counter logic part. It can be said that the important thing in memory design is synchronization between input data and the clock that can transmit the data. It is also important to synchronize with 32 enable signals generated through counter logic at the same time. Since numerous CMOS are included in the memory, it is important to prevent the supply voltage from degrading as the current consumption increases. In addition, since they are all dynamic switching circuits, the supply voltage is shaken a lot. To solve these problems, decoupling capacitors and power mesh layouts are used. Figure 4.1-1 shows the block diagram of the entire memory.

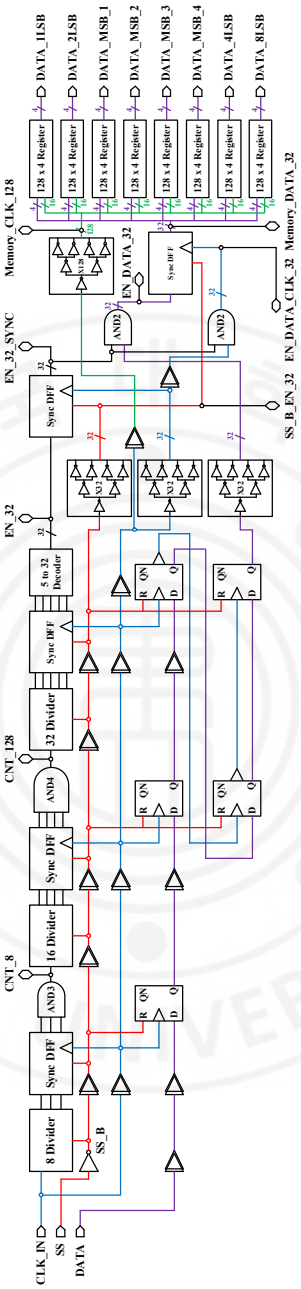

Figure 4.1-1 Entire Memory Block Diagram

4.1.3. Counter Logic in Memory

It is about counter logic used in memory. First of all, as mentioned before, data distribution is essential to create N parallel output through 1 serial input. Therefore, a signal that cuts and inserts data according to location is required, and in this memory, an enable signal plays a role. One parallel output consists of 128 bit register, with a total of 32 parallel outputs. At this time, a total of 128 x 32 (4096) bit of data are required to fill all registers in the memory, and it can be seen that the data must be divided into 32 pieces each of 128 bit. Therefore, the enable signal is a signal that must sequentially create 32 128 bit high-level signals.

The simplest way to create such a signal is to utilize counter (=frequency divider) and logic gate. At a particular frequency, 1 bit signal means data as much as one period of clock signal. The explanation of this is shown in Figure 4.1-2.

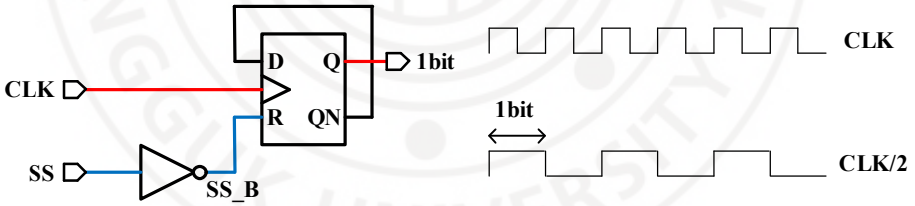

Figure 4.1-2 1 bit Counter and Timing Diagram

Therefore, it can be seen that a 7 bit counter is required to make one 128 bit signal. But since this memory needs 32 of these 128 bit signal, need more counter, a total of 12 bit counter. As shown in the figure above, it can be seen that the signal from the counter is half the frequency, and these signals are converted into appropriate enable signals through the logic gate, which is 5 to 32 decoder.

However, there is a point to note when designing a 12 bit counter. In general, a 1 bit counter can be designed through a DFF with a reset function, and it should be noted that the signal generated must have a propagation delay compared to the input. Therefore, since 12 bit counter at once without a synchronization circuit in the middle have a delay for each bit signal, there will be a lot of glitch, static, and dynamic hazard when such signals enter the logic gate. Therefore, in this memory, the counter is divided little by little and the synchronization circuit is used for each stage to minimize this risk. The comparative figure for this is shown in Figure 4.1-3.

The following is a description of the 5 to 32 decoder design. 5 to 32 decoder have 5 inputs of 128, 256, 512, 1024, and 2048 bit signals. Even if each bit signal is synchronized for each stage at a 12 bit counter, there is a risk of glitch and dynamic hazard because the delay that occurs additionally during the input interconnect connection of this decoder and the load of each signal are different. To solve these problems, a ground line is added between signal lines, and a synchronization circuit is included in addition the decoder output. This process is further described in the data part, and the schematic of 5 to 32 decoder is shown in Figure 4.1-4.

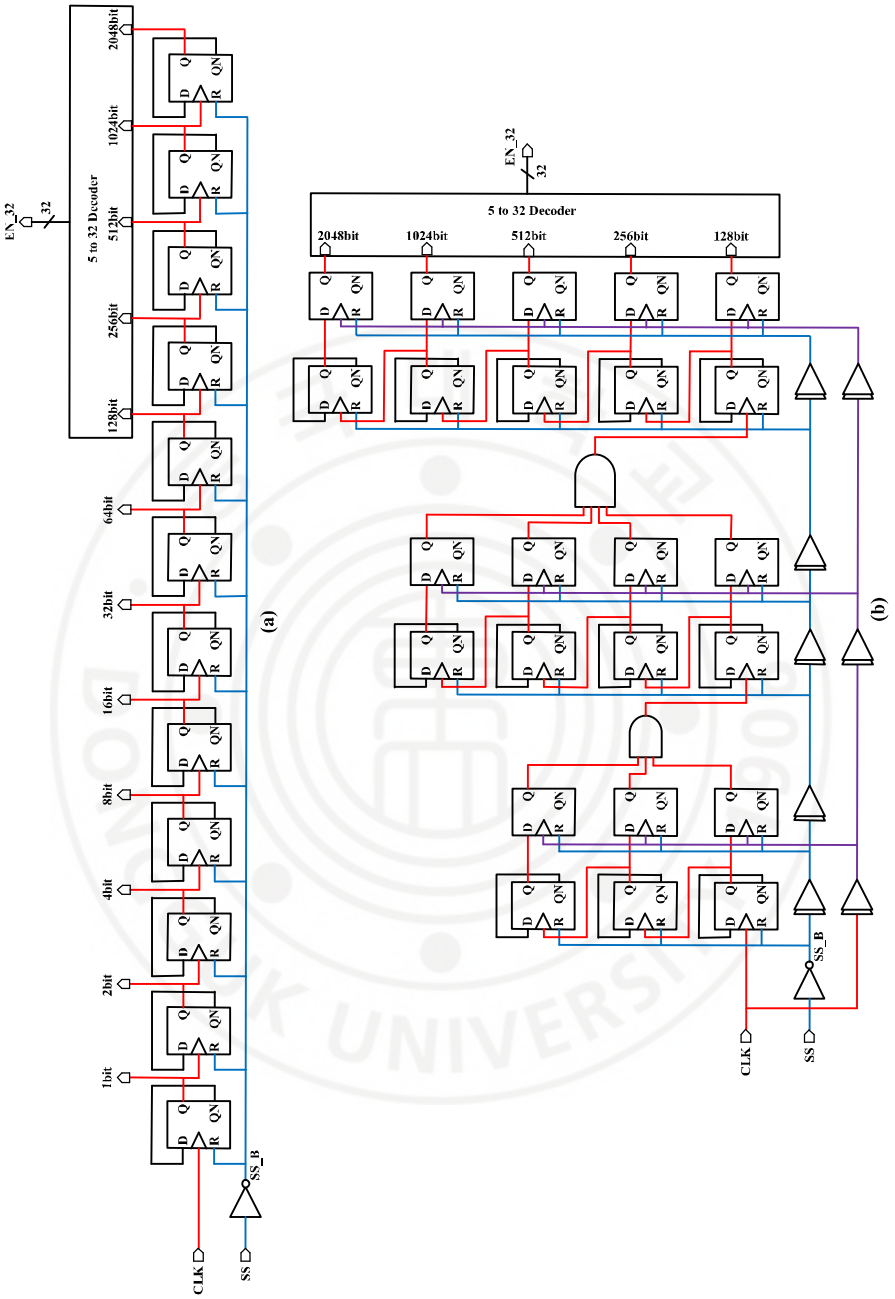

Figure 4.1-3 12 bit Counter Block Diagram (a) without Synchronization Circuit (b) with Synchronization Circuit

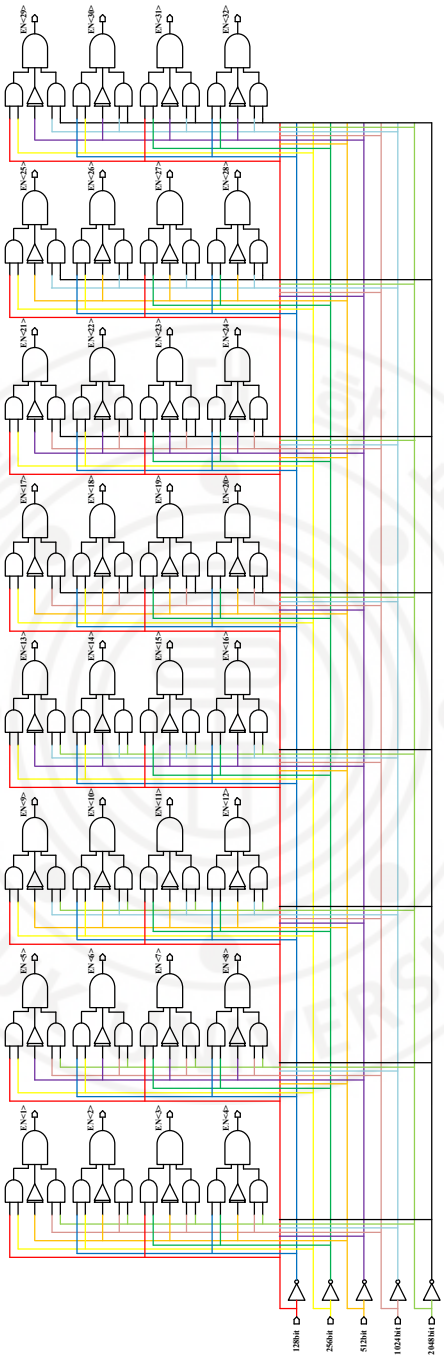

Figure 4.1-4 Schematic of 5 to 32 Decoder

4.1.4. DATA Register in Memory

This is a description of the transmission process of the DATA register except counter logic. As can be seen so far, it is impossible to convert to all parallel outputs at the same time with one serial input. In addition, a series of data stored in the register is a consumed value. Therefore, since it is impossible for one serial input to be reflected in the input of the DAC in real time, the design is carried out in a way that can repeatedly transmit only the data value while storing certain data. To do this, data circulation must be prioritized, and this method receives 128 bit of data in read (=enable on) situations and then continues to circulate 128 bit of data in write (=enable off) situations. In the write method, the timing of sending data to the DATA Interface is determined through SS and switch. Additional requirements in this situation include clock signals of the same timing for all registers, independent clock signals, and synchronization with data signals.

There is important point to consider in the process of designing a circulating DATA register. One register consists of a 128 bit shift register format, where the method of giving a clock signal should be considered. In order to circulate, there is a method of connecting the first DFF input and the last DFF output through a switch. If a 128 bit register is given a single clock signal, the clock on the first DFF and the clock on the last DFF have a great delay difference. The most important reason for this is that the difference in delay in the clock also means that the data applied to the DFF also has a phase difference. Then, when the data circulates at the end of the read

section and the write section begins, there is a difference between the data phase that the last DFF transmits to the first DFF and the clock phase of the first DFF. As a result, the 128 bit register cannot completely preserve the read data. Therefore, to solve this critical problem, 128 bit register is also separated into 4 arrays of 32 bit register, and a single clock signal is given separately for each 32 bit register.

This allows DFF on the same x-axis on the layout to have a clock signal of the same phase, and 128 clock signals of the same phase are required for the entire memory. It is implemented through a 129 clock tree circuit. The direction of the clock is always right, the direction of the data is right and left, and a buffer is added for each output data to make the delay of the clock smaller than the propagation delay of the data. The layout is constructed in the form of Figure 4.1-5, and as can be seen, it can be expected that the first DFF and the last DFF will take the same phase clock and data. The circulation method register is constructed in this way, and Figure 4.1-5 shows the differences between the two methods described above.

This is a description of the synchronization of the enable signal and signals entering the register. Synchronized enable signals, data, and clock signals are sent to the register's input DFF using the AND logic gate. At this time, it can be seen that the clock in the register and the clock in the input DFF are independent clocks, which enables more stable data transmission. In addition, the input DFF and register can be connected only in the read section, and only the internal register can be connected in the write section. The most important thing is that all data, enable signal and clock

signals are synchronized. Figure 4.1-6 shows the explanation of this.

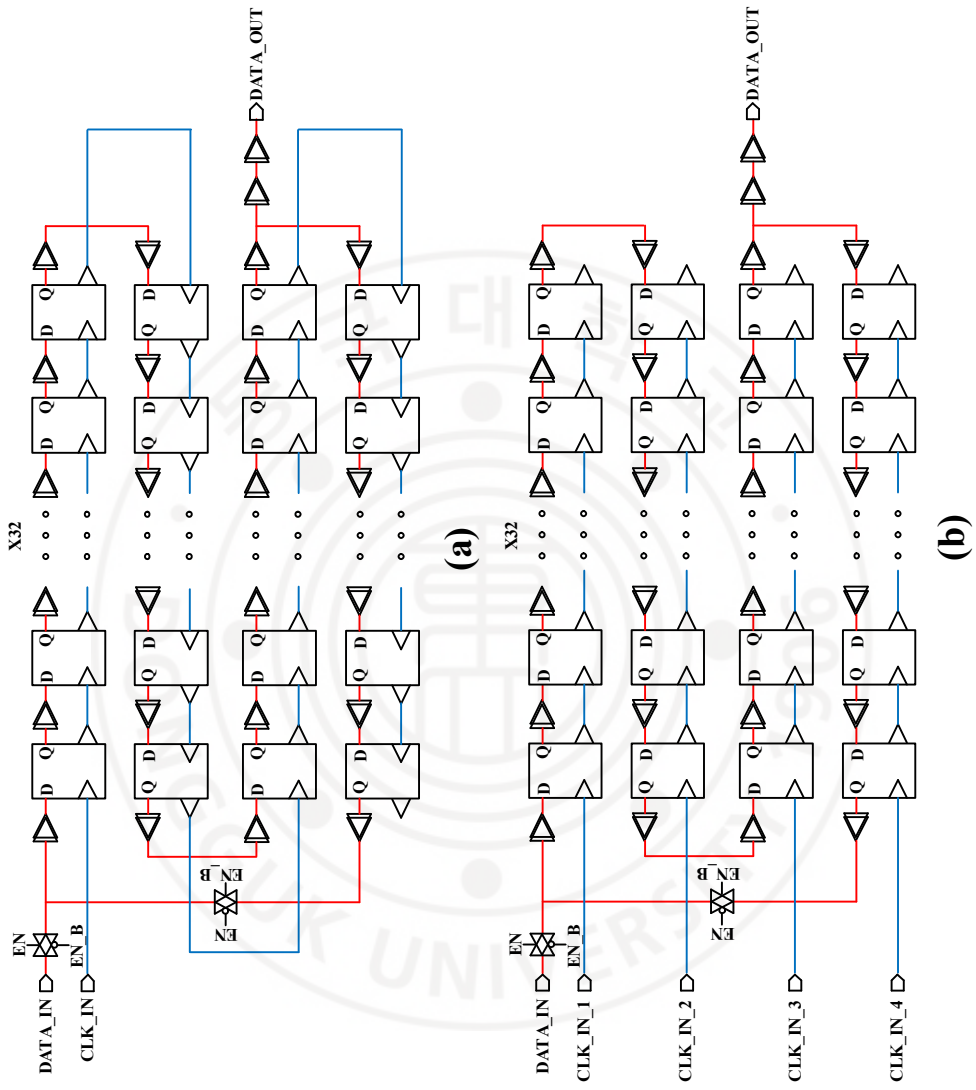

Figure 4.1-5 Block Diagram of 128 bit Register (a) single clock method (b) multiple clock method

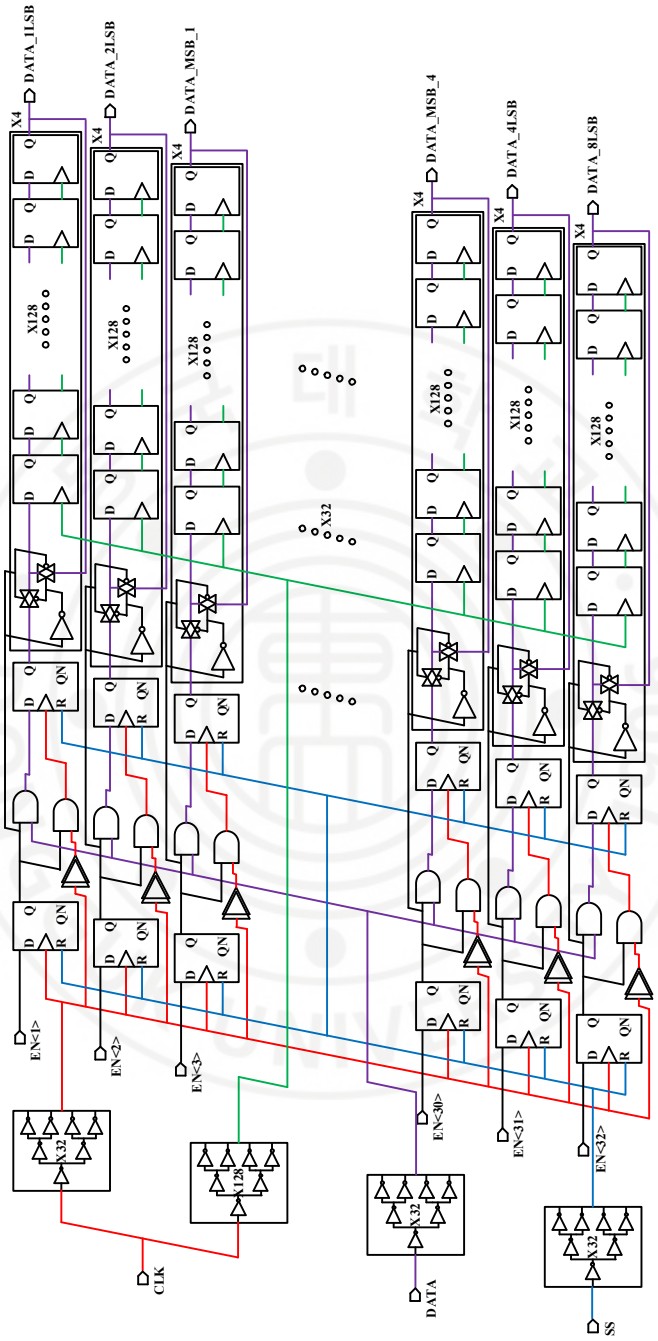

Figure 4.1-6 Block Diagram of Signal Transmission in Memory

Chapter 5 Time Interleaved Current Steering RF DAC Implementation

5.1 Introduction of Time Interleaved RF DAC

DAC is a system that has long been essential to the transmitter. With the development of the CMOS process, the operating frequency of the DAC is also increasing as the operating frequency of the digital domain is increasing. In addition, with the development of wireless communication systems, Direct Digital Synthesizer (DDS), which uses RF DAC instead of conventional complex transmitter methods, has a very simple structure. Accordingly, RF DAC requires high specifications because it is a system that replaces the existing complex transmitter structure. The DAC basically outputs an appropriate analog output according to the incoming digital data input. Therefore, the general principle of DDS is that DAC can output all modulated analog signals from low frequency (DC) to Nyquist frequency if digital data comes in correctly. Therefore, the ultimate goal is to design a system that can simultaneously interact with input data while reducing the effects of static and dynamic errors of existing DAC as much as possible. Since single-channel DACs have limitations in sampling rate, time interleaved structures using sub-DACs and analog multiplexers show potential for multi-channel DACs, and their research value is high because they are not yet active.

Before entering the actual DAC design, it is necessary to know and prepare for

the factors affecting the linearity of DAC. Factors affecting linearity are largely divided into static and dynamic errors. All of these errors need to be reduced to some extent to expect proper DAC operation. These errors can also be said to be errors corresponding to sub-DACs in Time Interleaved DACs (TI DAC), and do not include errors between sub-DACs and analog multiplexers. Static errors can be said to be errors at low frequencies, and can be largely divided into systematic errors and random errors. Dynamic errors can be said to be errors at high frequencies, and are basically related to timing, parasitic capacitance, and digital input code.

Systematic errors include graded errors due to the voltage drop of the supply line and symmetric errors due to thermal distribution, and to solve this problem, a switching scheme and a hard supply voltage line layout are usually used. In addition, there is a concept called finite output impedance, which affects the linearity of the DAC by changing the drain current due to the drain voltage change of the current source. This is mainly solved by using the cascode structure and the long length current source device, where all devices in the DAC must satisfy the saturation. Random error by current source device mismatch generally mitigates the impact through segmented structure and adjustment of dummy device, long length device, and overdrive voltage.

In the aforementioned static error, the analog amount and the parameters of devices are the main contents, but in the dynamic error, other contents are the main contents. However, even in dynamic errors, finite output impedance is a concept that

applies equally, in which case parasitic capacitance is additionally involved. This can also be referred to in conjunction with the digital input code, which means that the impedance of the DAC's differential output varies depending on the code and consequently affects the linearity of the DAC. This part is not a problem because the difference between the ideal 1 LSB current and the actual 1 LSB current can be sufficiently reduced if the bias point of each device is set to have a margin and the saturation is satisfied. However, it is natural that problems arise in the glitch and settling time parts due to the intervention of parasitic capacitance. This part is not considered to be a part that can be greatly improved as long as the parameters of the devices of the DAC are already determined.

Representative timing errors include imperfect synchronization of digital data and simultaneously turn off of a differential current switch. In the case of imperfect synchronization, it can be solved through a switch driver at the front end of the DAC switch, and the clock tree must be present as it operates at a higher frequency. When the differential switch is turned off at the same time, a discharge occurs in the source node voltage of the switch, and even if one switch is turned on again, a time to charge the node voltage is required, resulting in performance degradation. This is usually solved by using a method of making the crossing point of digital data entering the switch larger (NMOS) than or less (PMOS) than the turn-on voltage of the switch. TI DAC design is possible only after the following errors are first resolved in sub-DAC. In fact, the bias point with the analog multiplexer on top of the sub-DAC

should be considered while proceeding with the design.

The structure of the dual-channel TI DAC is generally composed of two sub-DACs and a 2-to-1 analog multiplexer. It has the advantage of being able to double the sampling rate with analog multiplexer, and thus reducing the burden of data interface. In addition, as the current of the sub-DAC can additionally have a time of 1/(Fs*2), stable output can be extracted. However, since an additional analog multiplexer needs to be included, there is a voltage headroom problem, and it is difficult to use a single supply. In addition, additional clock drivers and timing to fit the output of the sub-DAC are needed, and the complexity of the structure can be said to be a drawback. In the existing TI DAC paper, the analog multiplexer is operated in the deep triode region with the use of single supply, but in this thesis dual supply is used instead of single supply, and the TI DAC with analog multiplexer operating in saturation region is described.

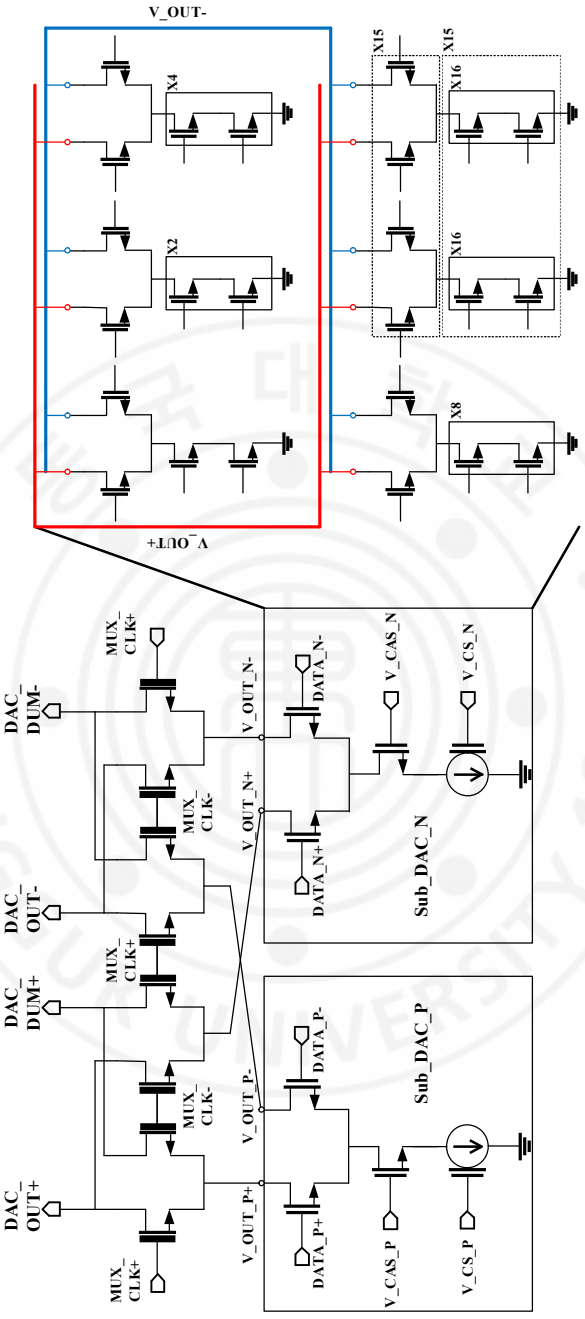

Figure 5.1-1 Time Interleaved Current Steering DAC Structure

5.2 Proposed Time Interleaved DAC Architecture

The composition of the entire TI DAC is as shown in Figure 5.2-1. Sub-DAC use a 4 MSB / 4 LSB segmented structure and configure a data interface accordingly. In this process, the design of the sub-DAC is conducted first, and the size of the data interface is adjusted according to the layout size of the sub-DAC. In the case of sub-DAC, it is difficult to change the layout size after designing the schematic and layout that meet the desired specifications, so it can be said that it is a more convenient way to adjust the digital circuits to the sub-DAC. Since the size of digital circuits must also be larger than the minimum size to operate at high frequencies, it is important to be careful because if the sub-DAC is designed too tight, all the data lines to the switch array may not be same. Also, the symmetry of the layout should be kept by default. There are two basic DAC layout methods, row and column method and current source array method. Since the row and column method has difficulty in the synchronization process of all data, it can be said that the current source array method is better, especially in DAC with high frequency.

A switching scheme is applied to the current source array with dummy device, and all 1 LSB current source is used to reduce device mismatch. The digital interface is largely composed of Decoder, DFF, MUX, and Switch Driver. Although not illustrated in the Figure 5.2-1, a clock tree is used at the front of all timing circuits to minimize data skew. It has a configuration for data transfer suitable for the 4 MSB / 4 LSB segmented structure, and two parallel decoders are required because 4 to 2

MUX is used. At this time, the decoder consists of 4 binary decoder for 4 LSB data and 4 to 15 thermometer decoder for 4 MSB data. After receiving a total of 16 Fs/2 sampling rate data from memory, converting it into 38 Fs/2 sampling rate data through a decoder, there are 38 DFF array to match the edge of each data. Even at this time, the supply height of the layout is designed in the same way to make the line that transmits each data the same. Due to the nature of the TI DAC, two sub-DACs must contain Fs sampling rate data with a 180 degree difference, so these data are generated through clock of opposite phase in the DFF array after 4 to 2 MUX. The latch array at the front of the switch array is constructed using a high crossing point latch, where clock of opposite phase are inserted respectively. When digital data suitable for the switch of the two sub-DACs enters, the above analog multiplexer acts to allow the output of the sub-DAC to flow according to the phase of the clock, where the analog multiplexer is configure using a 1.5 V device. The full scale current of this TI DAC is set to 4 mA, so the single output voltage swing is 200 mV, and the 1 LSB unit current is 15.6 μA.

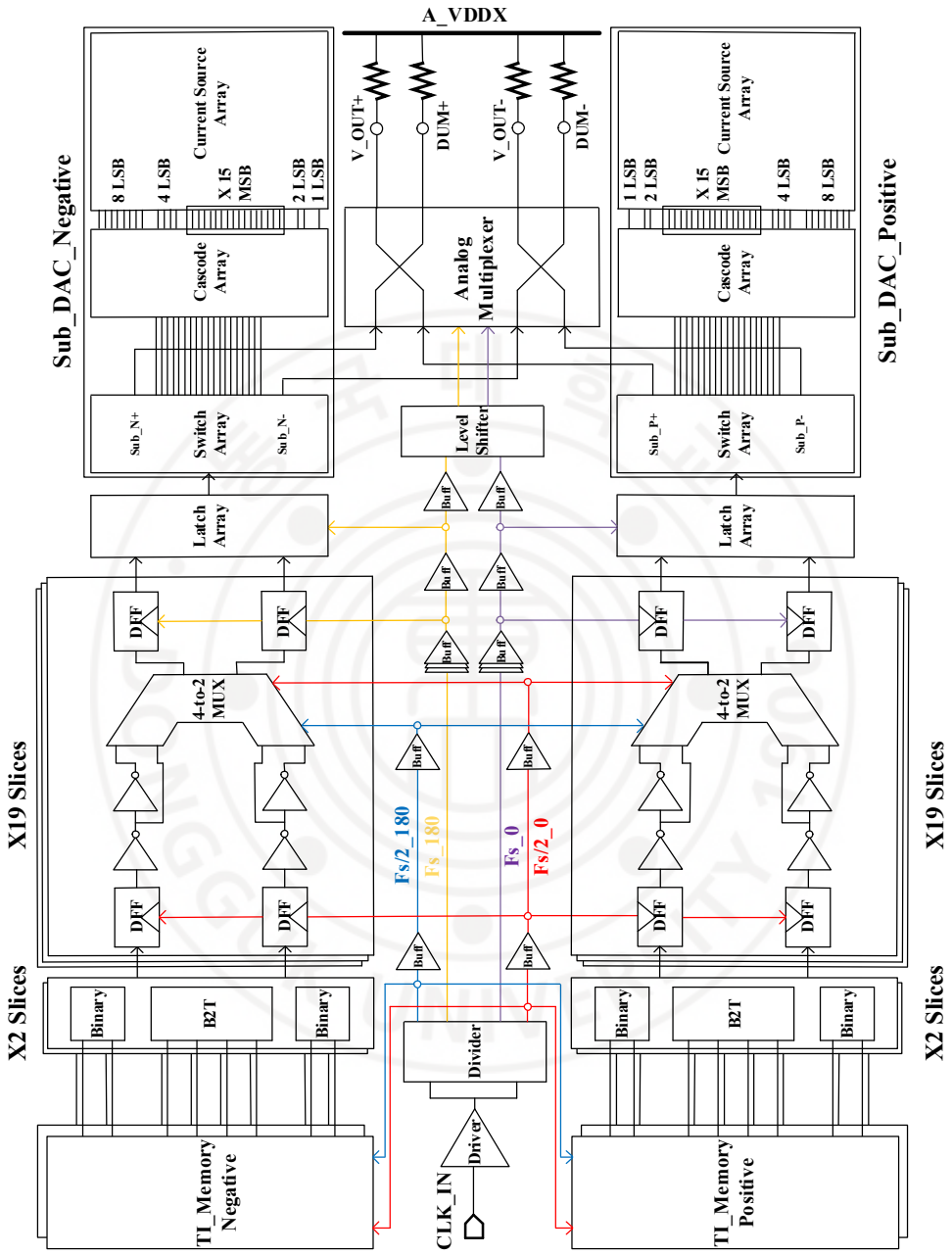

Figure 5.2-1 Entire Time Interleaved Current Steering DAC Block Diagram

5.3 Circuit Implementation

This DAC is designed in the Samsung 28 nm process, and a twin-well NMOS device is used due to the area problem. In addition, it is designed in a full custom method, and the full scale current is 4 mA using 1 LSB current of 15.6 μA.

5.3.1. Sub-DAC & Switching Scheme

Due to the development of the CMOS process, the analog supply voltage is scaled and gradually decreasing, so it is difficult for all devices of the DAC to extract a desired current stable while satisfying the saturation. In addition, the overdrive voltage of the current source cannot be lowered indefinitely because it directly affects the device mismatch and size. Accordingly, the design should be carried out in consideration of both the voltage headroom problem and saturation region operation in DAC, so the sub-DAC uses the lvt device. The device size is determined using the existing yield formula and designed with a certain margin. In addition, 1 CS + 1 CAS structure is used to reduce mismatch through the unity of the current source as much as possible, and the upper LSB and MSB except 1 LSB are used by configuring the 1 LSB unit CS + CAS structure as parallel.

The presence or absence of an analog multiplexer in the aforementioned voltage headroom has a greater impact. TI DAC with a 4 cascode structure has a more severe voltage headroom problem, and in other papers, the problem has led to an analog multiplexer driving in deep triode region. This TI DAC has a margin at the sub-DAC below and uses dual supply to operate all devices in the saturation region.

The voltage headroom of the basic CS DAC and TI DAC can be expressed as shown in Figure 5.3-1. In this thesis, the analog multiplexer is designed as a 1.5 V device for saturation operation. However, in this case, since the 1.5 V device has a larger Vth than the basic device, the required overdrive voltage is large. Therefore, TI DAC needs to design a sub-DAC accordingly as the voltage of each node decreases compared to CS DAC.

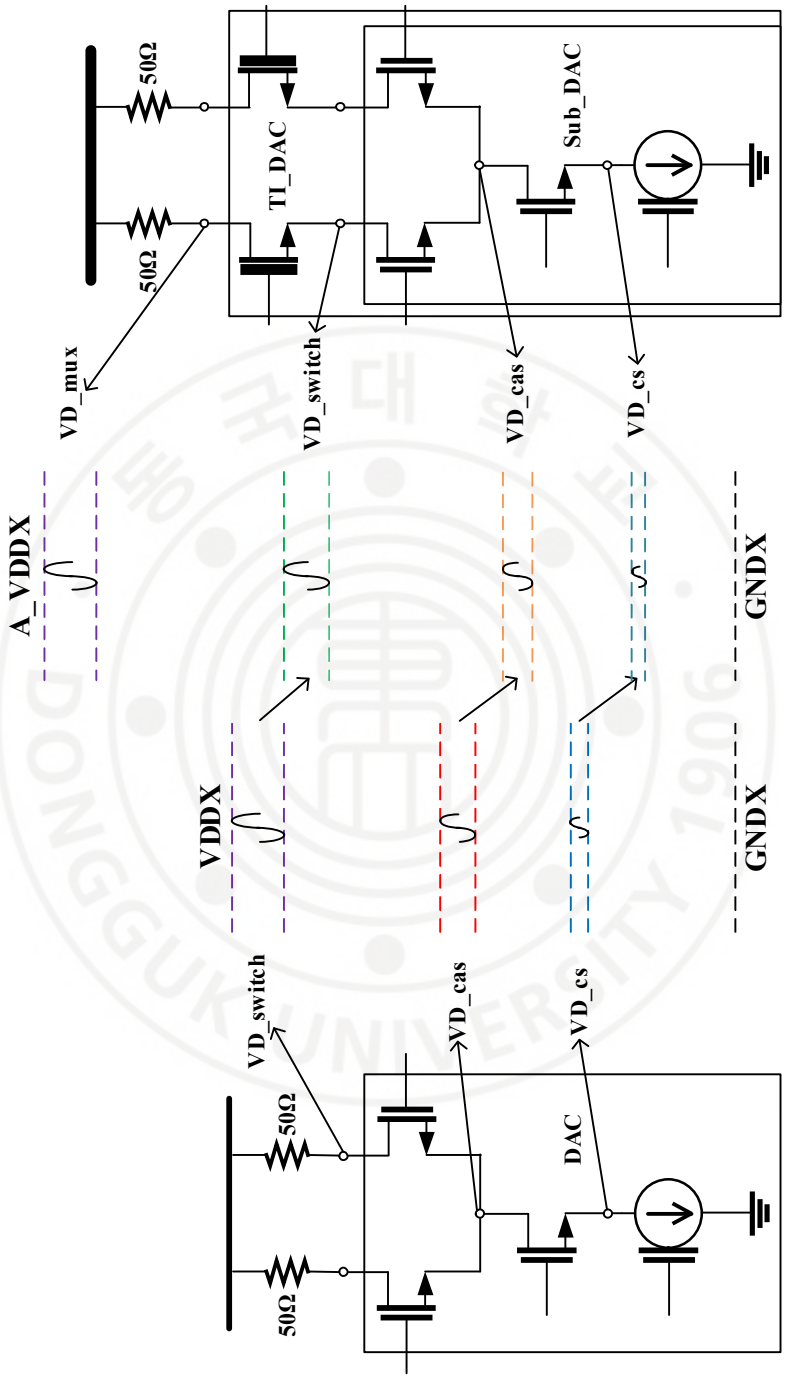

Figure 5.3-1 Voltage Headroom Comparison between CS DAC and TI DAC

The configuration of the sub-DAC is shown in Figure 5.3-2. The current source array is designed to reduce mismatch between current sources by placing 16 x 16 current source array and 2 columns and row dummy devices around them, and to facilitate signal line connections to cascode and switch array. In addition, the current source array is composed of 1 LSB unit current source, and the switching scheme is applied. At this time, one additional current source is not used. LSB current drives with 15 number current sources, and MSB current drives with current sources corresponding to each number.

In the current source array layout, the graded and symmetrical error are alleviated to some extent through the Q^2 random-walk switching scheme, but the errors cannot be supplemented in the upper switch array and the cascode array. To solve this problem, a hierarchical switching scheme is applied to the switch array that receives data. At this time, the cascode array and the data order inside the data interface are also designed according to each number. However, as can be seen in Figure. 5.3-3, since the number of MSB is not even, it is not complete compression in the case of symmetric error.

After configuring a current source array through the switching scheme, the current direction of all lines is designed to be the same, as illustrated in Figure 5.3-3, in the process of connecting lines with a cascode array. Accordingly, interference occurs only between current in the same direction, and interference between current in opposite direction is minimized. Here, the current in the downward direction

passes to the left and the current in the upward direction to the right, and the distance between the lines in the opposite direction is far enough.

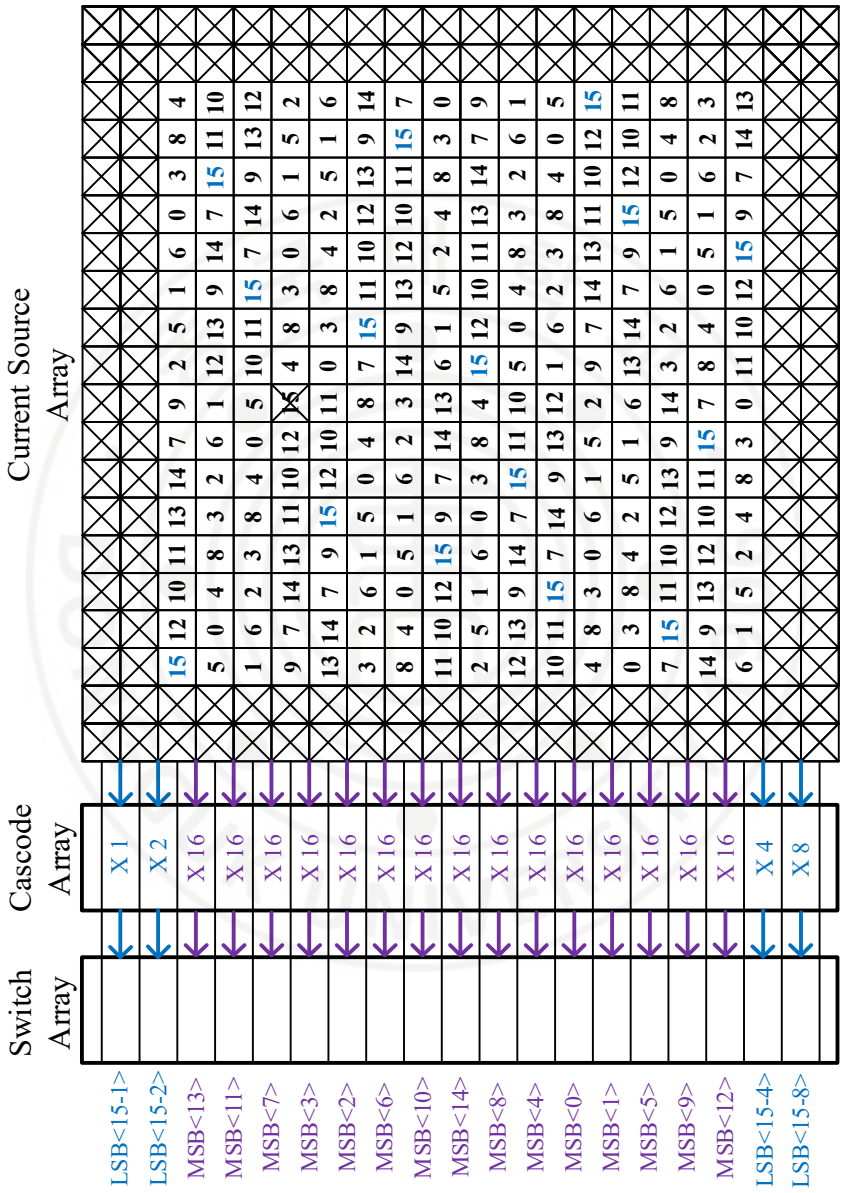

Figure 5.3-2 Sub-DAC Structure with Q^2 Random-Walk Switching Scheme

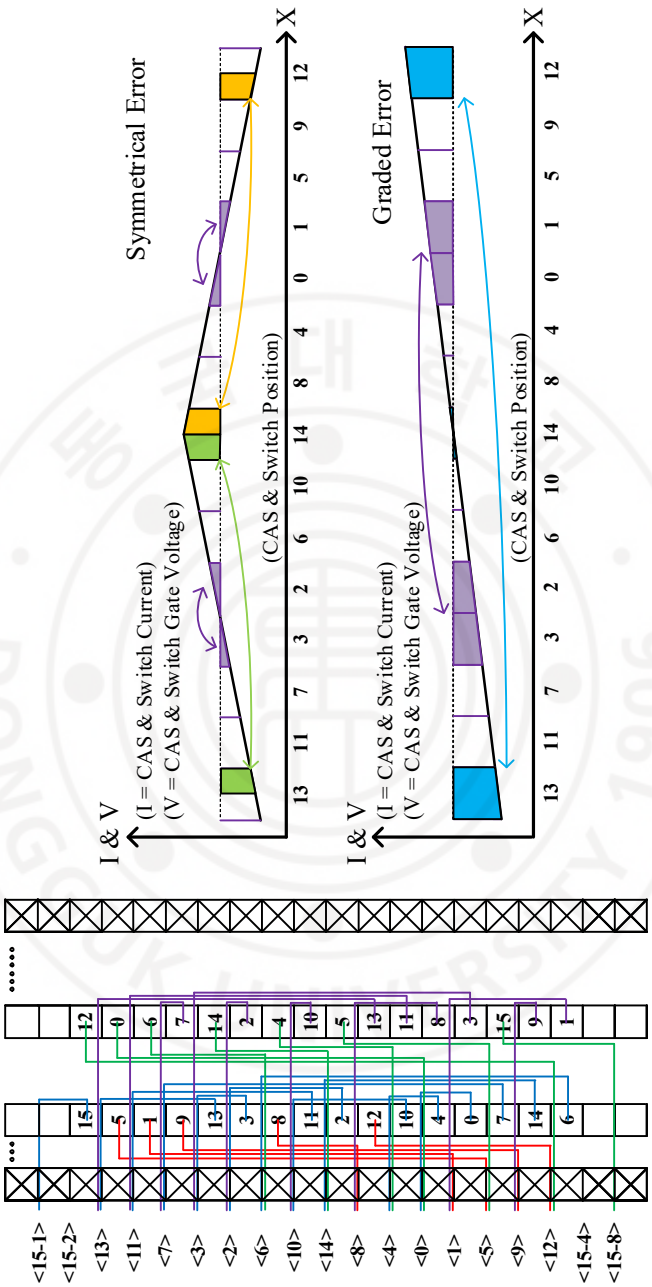

Figure 5.3-3 MSB Connection Method & Hierarchical Switching Scheme used in TI DAC Switch & Cascode Array

5.3.2. Analog Multiplexer & Timing Diagram

In designing a TI DAC, it is important to be clear about the differences from the basic CS DAC. TI DAC seems to be a simple structure with analog multiplexer on top of the basic CS DAC, but as this multiplexer is added to the actual design, there are many considerations. The differences between the two are simply shown in Figure 5.3-4 and Figure 5.3-5. The biggest difference is that the current switch of the basic CS DAC flows a fixed current according to position, while the output current switch (MUX switch) of the TI DAC flows from zero to full scale current.

Analog MUX requires a single MOS device to cover zero scale to full scale current, so unlike the basic CS DAC, saturation operation of all devices in all regions in impossible. Nevertheless, except for the low code region, it is designed accordingly using points that can be operated in the saturation region. The problem can be solved by adding bleeding current to each source of the analog multiplexer if the voltage points of each node of the TI DAC are well held. However, this paper does not cover that part. This point is also a different point of view because unlike previous papers, the analog multiplexer is used as 1.5 V device.

Since the analog multiplexer is used as a 1.5 V device, it is difficult to operate in the deep triode region like previous papers. This is because the Vth of the 1.5 V device is large, and the size of the device must be very large to operate in the deep triode region. When the size of the device is increased, it is very difficult to drive the clock to the MUX, and in addition, there are problems such as linearity, settling time,

glitch, and the like. Therefore, in this paper, it operates in the saturation region, and accordingly, it is designed with margin by lowering the voltage point of the 3 cascode device nodes below.

Figure 5.3-5 shows the timing diagram of the TI DAC. In this thesis, the circuit for driving the clock to the analog multiplexer is designed with reference to [21]. In designing an actual TI DAC, it is important to make DATA and CLK satisfying the following timing. It is also important to ensure that the MUX switch is not turned off at the same time as the switch of the basic CS DAC. Therefore, since the MUX clock must also be a high crossing point clock, the voltage point of the 3 cascode device nodes below is lowered.

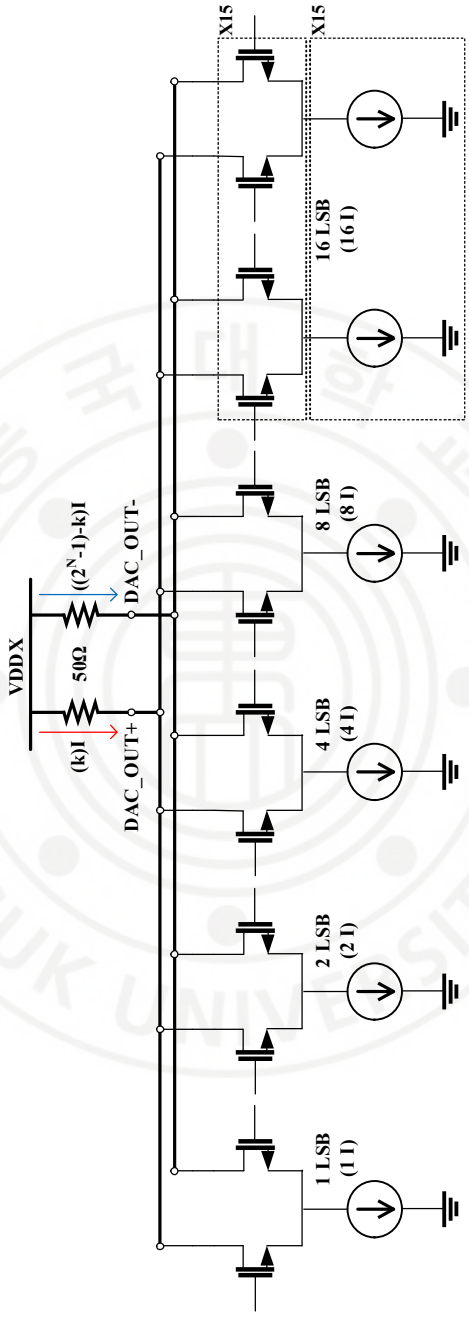

Figure 5.3-4 Simple Basic Current Steering DAC Structure

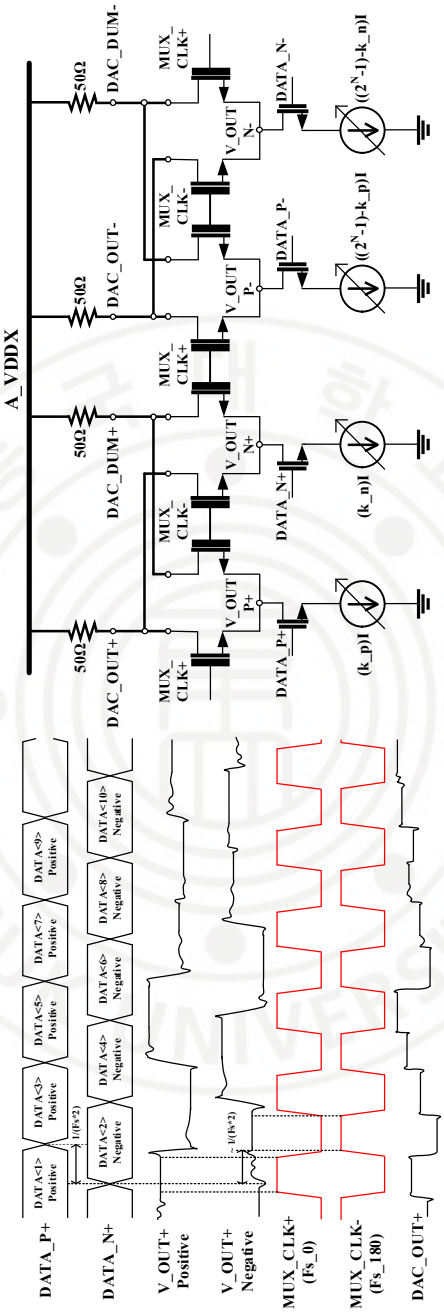

Figure 5.3-5 Simple TI Current Steering DAC Structure & Timing Diagram

5.3.3. DATA Interface

This part is a description of DATA Interface, which makes data coming from memory into data entering DAC. Designing a DAC analog parts are important, but digital parts that serve to deliver the data that the DAC analog part needs are also important. All data entering the DAC current switch must be synchronized to reduce timing related errors. Therefore, it is important to arrange the data through a timing circuit every time. It is also important to ensure that all data lines and circuits do not differ through a symmetric layout. In this design, the layout of the DATA Interface is designed so that it can be connected in a straight line according to the height of the sub-DAC switch.

The circuit that first receives data from the memory is the decoder part. In reality, data from memory is also sorted through DFF, but this part is omitted. Figure 5.3-6 is a 4 to 15 binary to thermometer decoder circuit. As the hierarchical switching scheme of the sub-DAC switch is applied, the data is also placed in the appropriated order. Buffers in the input signal line transmission are placed to reduce the load burden, which becomes more severe as the frequency increases. In addition, there is a problem in this part that it may be difficult to obtain an accurate value due to the glitch caused by static and dynamic hazard. Therefore, with the buffer of the input signal line, the dynamic hazard problem is alleviated by the ground line between signal lines to prevent crosstalk. It also alleviates the static hazard problem by adding a buffer to meet the delay of the logic gate.

Since the data coming out of the decoder is not actually aligned, it is important to sort through the FF first (due to the delay difference between the line and the buffer). Then, increase the sampling rate using 4 to 2 MUX, and then make data entering the DAC through FF and latch. Since digital parts consume the most power in DAC, decoupling capacitors and power mesh layouts are required.

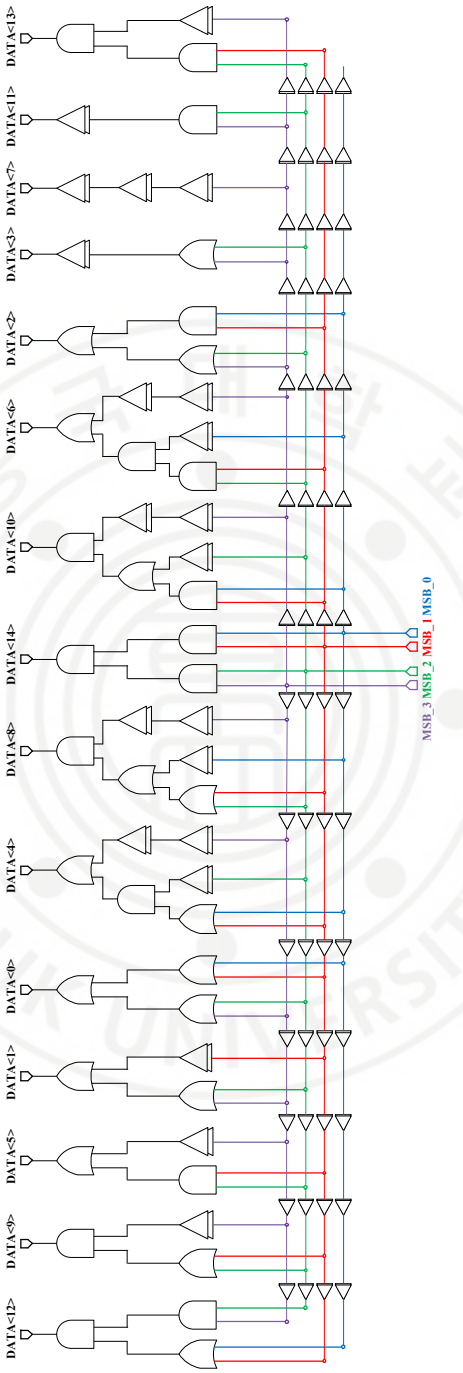

Figure 5.3-6 Schematic of 4 to 15 Binary to Thermometer Decoder

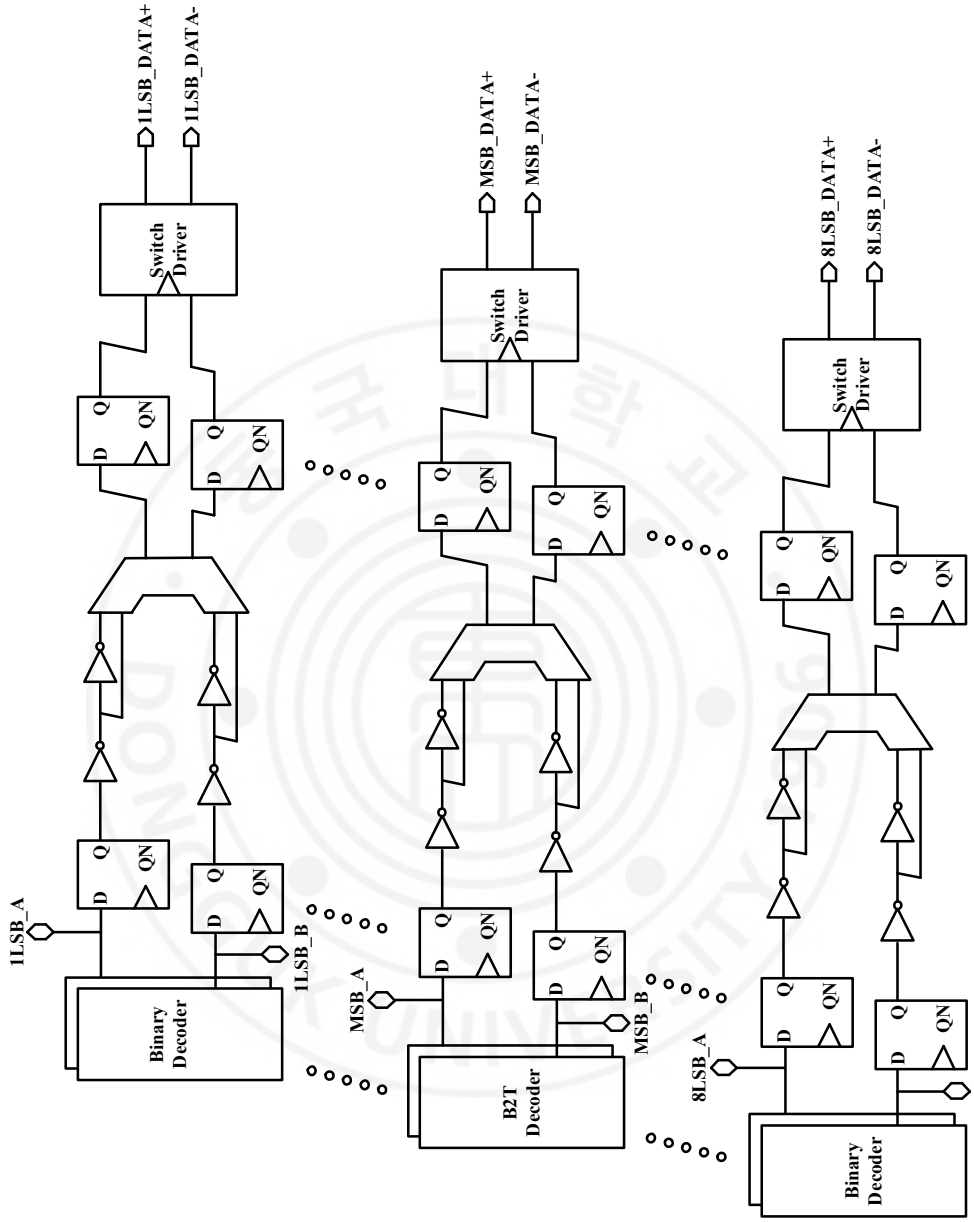

Figure 5.3-7 Block Diagram of DATA Interface

5.3.4. Clock Distribution

The number of data required for the DAC is determined according to the resolution and segment degree of the DAC. Accordingly, the number of circuits required for the DATA Interface is also determined. Just as it is important to sort the data through the DATA Interface, it is also important to get the necessary clock signal in time. This is a more important problem as the frequency, so it should be carefully considered and designed.

Since there are so many circuits that require a clock in the DATA interface, driving a lot of load through a signal clock is impossible at a high frequency. Therefore, a clock tree is required, and an appropriate clock is inserted into each circuit. However, the output of the clock tree is also difficult to make zero skew, and if the layout is not good, the skew becomes worse. Theoretically, the clock tree for perfect timing must satisfy the output of the 2^N. However, in this case, it is difficult to satisfy the conditions in a DAC using a segmented or thermometer structure excluding a full binary DAC. Therefore, as shown in Figure 5.3-7, a clock tree with less skew is designed by adjusting the dummy inverter and line length.

Since the clock signal used in the DAC has to drive a lot of load, the clock tree is absolutely necessary, and the proper timing alignment of the signals is required. For perfect timing each clock signal, the clock tree must satisfy 2^N. In the case of a DAC using a segmented structure, it is difficult to satisfy this condition. Therefore, the timing is adjusted by adjusting the dummy inverter and line length.

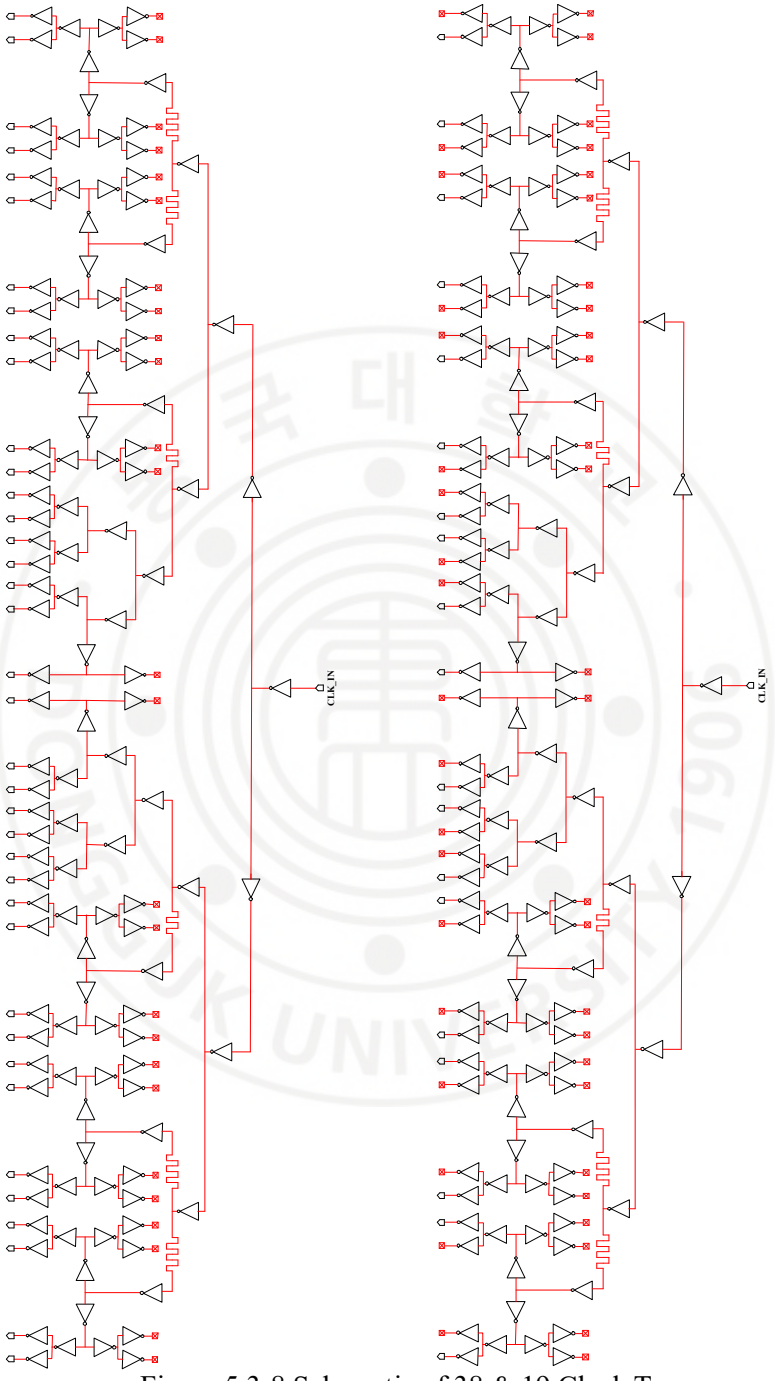

Figure 5.3-8 Schematic of 38 & 19 Clock Tree

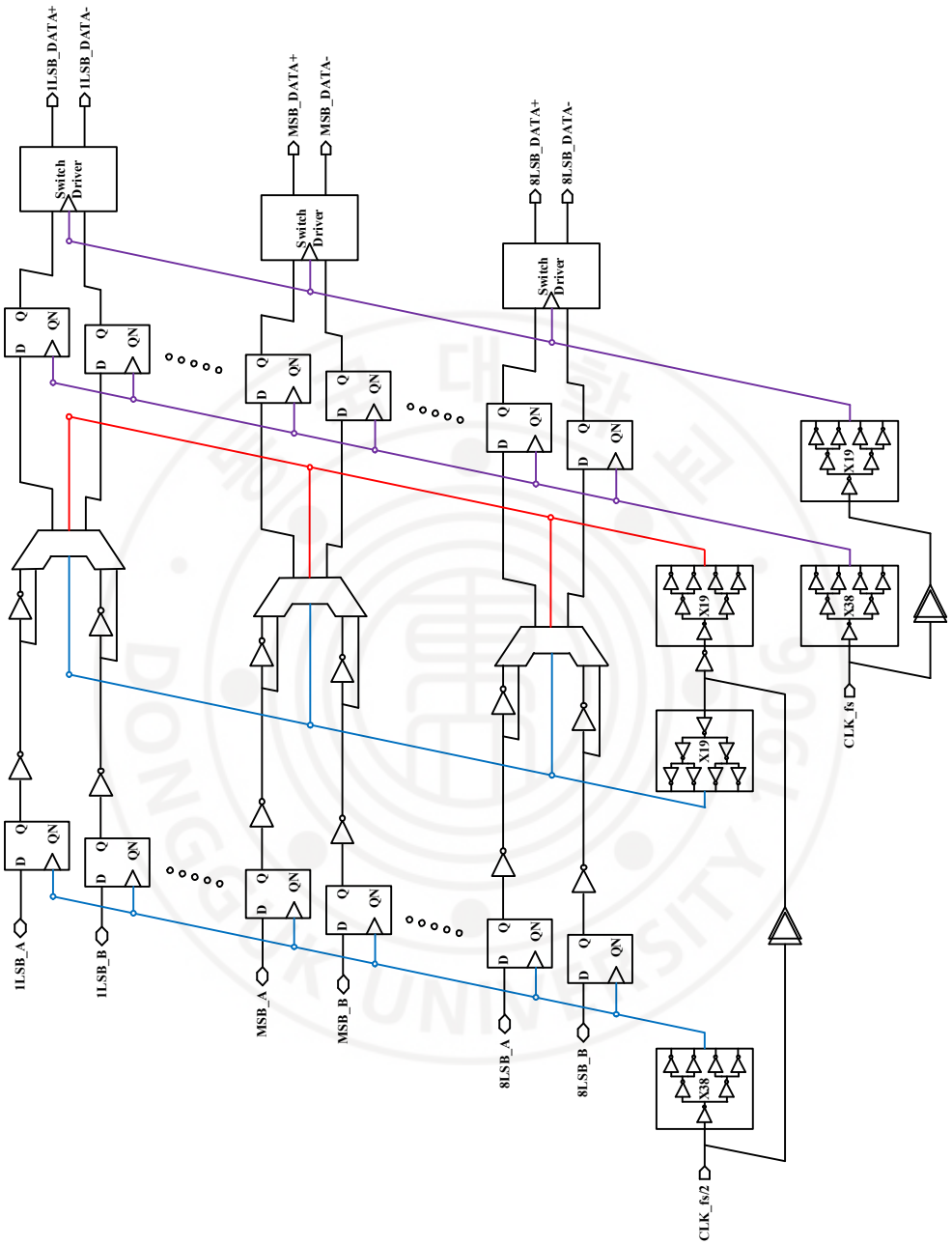

Figure 5.3-9 Block Diagram of DATA Interface with Clock Tree

5.4 Simulation Results & Measurement Setup

It is about 28 nm TI DAC simulation results and measurement setup. Figure 5.4-1 shows the TI DAC digital code 1 LSB shift post layout simulation result. At this time, the sampling rate of the TI DAC is 8 GS/s. It is possible to check 200 mV output swing from 1.5 V to 1.3 V according to 4 mA, which is a full scale current.

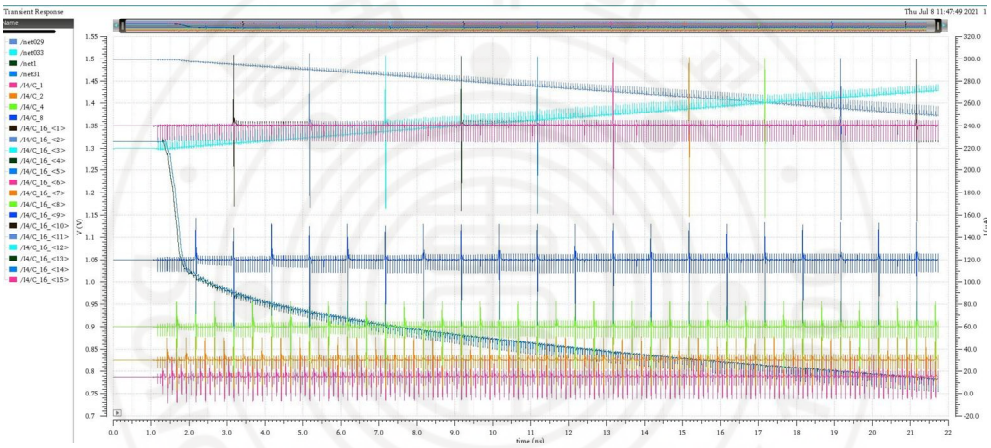

Figure 5.4-1 TI DAC Digital Code 1 LSB Shift Post Layout Simulation

Figure 5.4-2 shows the actual TI DAC chip and layout. Signals other than clock, and output are inserted using wire bonding and PCB. The size of the chip is 2.1 mm x 1.7 mm.

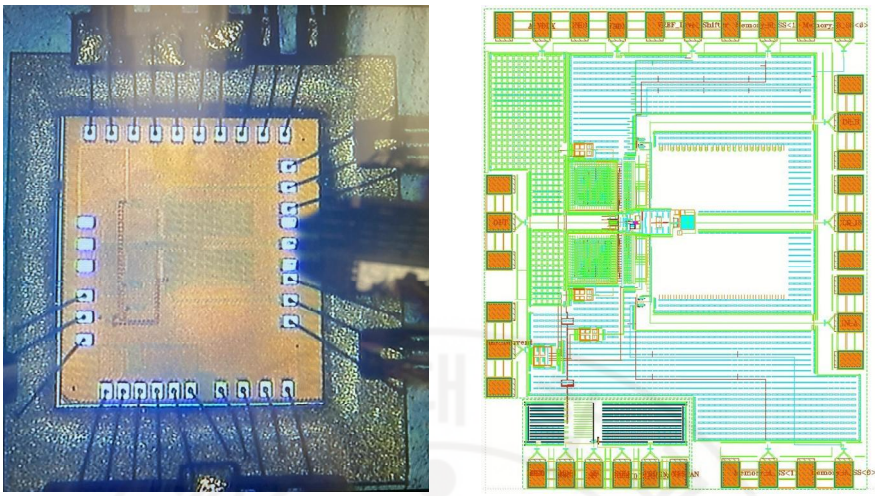

Figure 5.4-2 TI DAC Chip and Layout

Figure 5.4-3 shows the TI DAC measurement setup. The clock signal uses a signal generator to put 4 GHz clock, and the data signal uses AWG to put 1 GS/s data. The output of the TI DAC is checked through an oscilloscope.

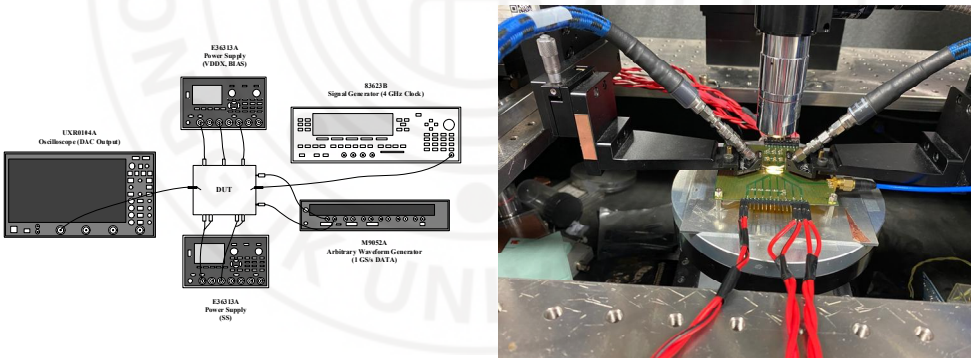

Figure 5.4-3 TI DAC Measurement Setup

Chapter 6 Current Steering RF DAC Implementation

6.1 Introduction of Current Steering RF DAC

This chapter contains the method and related theoretical contents of designing the actual Current Steering RF DAC (CS DAC). There are many considerations when designing CS DACs that operate at high frequencies. In fact, there is an additional part to be done in layout design, and although it is the same at low frequencies, timing between clock signal and data signal becomes more important at high frequencies.

In fact, the most important part of the design is how much voltage each node in the CS DAC will be set. In addition, this is more important and difficult in a state where supply voltage scaling of the CMOS process is currently underway. A typical CS DAC is a structure with a 3 cascode device between GNDX and VDDX. At this time, in the case of VDDX supply voltage, the Samsung 28 nm process is 1 V and the TSMC 40 nm process is 1.1 V. All 3 cascode devices must satisfy the saturation region, and the drain voltage (=CS DAC output voltage) of the top switch device requires a space equal to the (full scale current * output resistance). Therefore, it can be seen that the voltage headroom problem increases as the full scale current increases, and the actual layout size is also considered.

The format of the 3 cascode device used in this thesis is based on the 4 LSB and 4 MSB segmented structure, and 1 MSB core consists of 1 x 16 unit LSB current

source + 1 x 16 unit LSB cascode current source + 1 MSB switch. This is to reduce the mismatch in each current source and in each cascode current source as much as possible. In addition, in this CS DAC, use Deep N-Well (DNW) device to reduce mismatch and to allow stable current flow through the use of independent GNDX. Although the size increases in terms of layout, it has an advantage in terms of capacitance by connecting the cascode current sources and switches each body voltage to the each source voltage.

All CS DACs begin by determining the amount of current, overdrive voltage, drain voltage, and device parameters of the current source. The most important considerations at this point are overdrive voltage and device parameters. This is because the mismatch between the current source devices is determined to some extent by the overdrive voltage, and the current safety of the current source device is determined by the L value of the device parameter. Theoretically, the higher the overdrive voltage and the longer the length of the device, the better the linearity of the CS DAC. In reality, the higher the overdrive voltage, the higher the drain source voltage required for the device to be in the saturation region, so there is a problem in terms of voltage headroom. In addition, as the length of the device increases, the device layout size increases, and if a high full scale current is required, the width also increases, and the capacitance value of the current source device increases, making it impossible to use it for a high frequency CS DAC. Therefore, it is important to find an appropriate value for the actual design, and the overdrive voltage

is 150 mV and the device length is 2 μm for the designed CS DAC. It should also be considered, and importantly, when the overdrive voltage and drain source voltage are fixed, there is only one parameter of the device that allows the desired current to flow.

Now, on top of the current source device are the cascode current source and the switch device that increase the impedance of the current source. At this time, increasing impedance is similar to saying that it can keep the drain voltage of the current source device small. However, this is the situation when the above devices also satisfy the saturation region. Therefore, the criterion for determining the parameters of the cascode current source and the switch device is the saturation region, and the smaller the size of the device, the better. In this case, it is recommended to determine the voltage point and parameter that can drive the amount of current flowing from the current source below in the appropriate point for the 2 devices above. In fact, CS DAC is this thesis uses all the same unit devices up to the cascode current source, so a method of adjusting switch turn on voltage, crossing point to improve performance is used. This will be explained later.

After the design of the CS DAC is completed, the next step is to design a DATA Interface that will carry the data to the CS DAC's switch. The most important thing in designing the DATA Interface is to create a stable high and low level voltage. When the frequency of the sampling rate and clock of the actual data increases, the GNDX (=low level) and VDDX (=high level) become unstable. Therefore,

decoupling capacitor and power mesh layout are essential, and the contents of this will be described later. Above all, this stable data is needed because the switch of CS DAC is an analog switch, not a digital switch. This means that the amount of voltage entering the switch from DATA Interface affects the current of the CS DAC as a result. As such, the DATA Interface also plays an important role in the CS DAC system as much as CS DAC.

Above all, the Current Steering RF DAC does not have much performance improvement. The reason is that, after the parameters of all devices of the CS DAC are determined, the operation of the CS DAC is always determined by the capacitance and parasitic capacitance of the device and does not change. Therefore, there are few ways to improve the performance of CS DAC internally, mainly by changing the outside to improve the performance. However, in this thesis, it is confirmed through simulation that the performance is improved by controlling the inside of CS DAC, and two methods are presented.

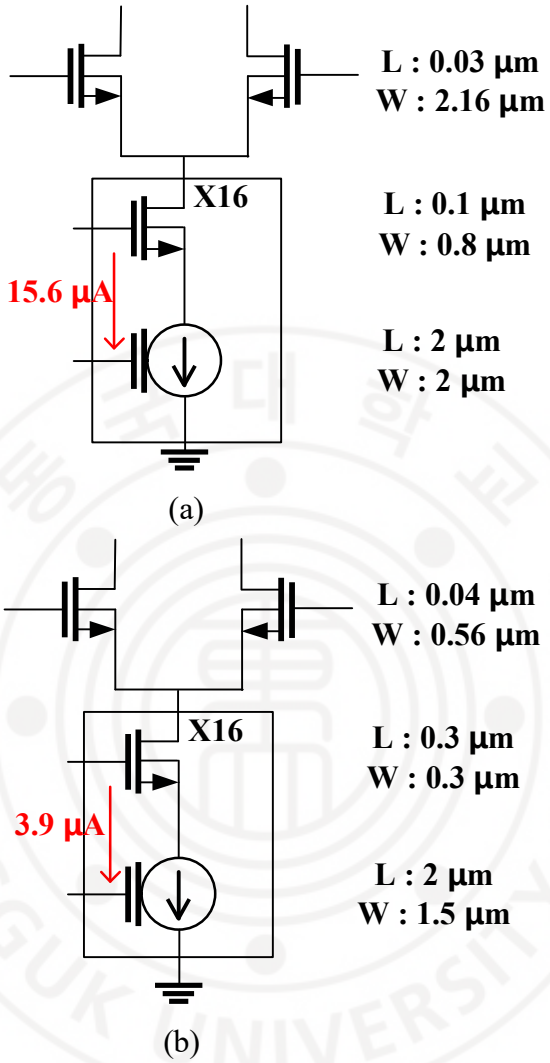

Figure 6.1-1 CS DAC 1 MSB Core Parameter (a) Samsung 28 nm (b) TSMC 40 nm

6.2 Proposed Current Steering RF DAC Architecture

It contains a rough description of the entire CS DAC that is actually designed. The CS DAC, designed in Samsung 28 nm and TSMC 40 nm, consists of almost the same structure. First of all, the 4 to 1 interleaving structure is used, and the Samsung

28 nm CS DAC target sampling rate is 16 GS/s and the TSMC 40 nm CS DAC target sampling rate is 12 GS/s. Unlike the before TI DAC structure, by using the 4 to 1 interleaving structure, more digital cells are required in the DATA Interface and Memory, which causes additional problems. CS DAC designed in TSMC 40 nm is designed by supplementing problems arising from Samsung 28 nm CS DAC designed previously. Both CS DACs use DNW devices for analog cells.

6.2.1. 28 nm Current Steering RF DAC Architecture

First of all, this is a description of the 28 nm CS DAC. Memory, DATA Interface, and Clock Distribution are drive by Digital VDDX, and CS DAC is driven by Analog VDDX. The aforementioned change in the interleaving structure doubles the number of digital arrays of the DATA Interface and Memory, adding at least two stages. In addition, one additional frequency divider is required in the clock distribution process. The actual design process is performed by designing the CS DAC analog part first and then adjusting the layout of the digital part of the DATA Interface to the analog part exactly. The reason for this is that the layout size of the analog part should be as small as possible to reduce the impact of additional parasitic capacitance. However, the disadvantage of this method is that as the degree of interleaving increases, the layout size of the digital part doubles and increases, which can cause area problems. Reducing the digital cell parameters of the digital part is also a method, but it is impossible because it requires some wide width to operate at an actual high frequency. In addition, it is also impossible to reduce the width of the

supply line because the supply line of the digital cell also operates at a high frequency and requires a wide width to minimize the voltage drop. Therefore, as the degree of interleaving increases, it becomes difficult for the digital part to accurately fit the analog part, which causes additional problems, so be careful.

It is about the delivery of 28 nm CS DAC DATA. A total of 128 x 32 (4096) bit of 4 GS/s data are serialized in memory, and a total of 32 repetitive 128 bit of data are generated. These data enter the decoder that generates the data needed for the switch of the CS DAC, at which time the output is a total of 76. Since the outputs of the decoders have different delays, they are then aligned through 76 DFF arrays on the next stage. At this time, a clock tree circuit exists in all stages of the DATA Interface. The sorted data is upconverted to 38 differential pair 8 GS/s 256 bit data via 4 to 2 MUX. After that, the alignment process is performed through 38 DFF arrays. It is upconverted to 19 differential pair 16 GS/s 512 bit data via 4 to 2 MUX again. Next, after alignment through a DFF array, data is transferred to the CS DAC through a high crossing point latch (=switch driver). At this time, the delay is adjusted so that all clocks enter each digital cell array according to the timing.

It is about 28 nm CS DAC Analog part. As mentioned earlier, all cells in the analog part use a DNW device. Therefore, although the area is larger than that of CS DAC that uses a general device, it is used because it has advantages such as stable current and capacitance reduction due to mismatch reduction. The DNW structure has less mismatch than conventional devices because the same N-Well, Deep N-Well,

and P-Sub Contact exist around all active NMOS. Therefore, it can allow a more stable current to flow, and it can be said that the current source upper devices have performance gains as the capacitance decreases as much as the Csb. For a more stable current, it is necessary to reduce the systematic mismatch. Therefore, in this CS DAC, the ground line of the current source array is tightly designed from the perspective of static performance rather than the perspective of dynamic performance. In addition, a switching scheme is used additionally, and this part will be explained later. In layout, the current source array uses 16 x 16 arrays, one of which is not used. In addition, an additional 2 x 2 row column dummy devices are added outside the array, which is the result of considering the mismatch and layout design. Next, the cascode current source array is designed based on the MSB, and a total of 16 devices are located, 8 above and below the lines from the current source array. The total is 8 x 38 array, and devices not used in the LSB part are set as dummy devices. Finally, a differential pair switch is located in the switch array at 1 x 19 array. In addition, A_VDDX used for output is supplied at an individual voltage different from other VDDXs for stable voltage supply.

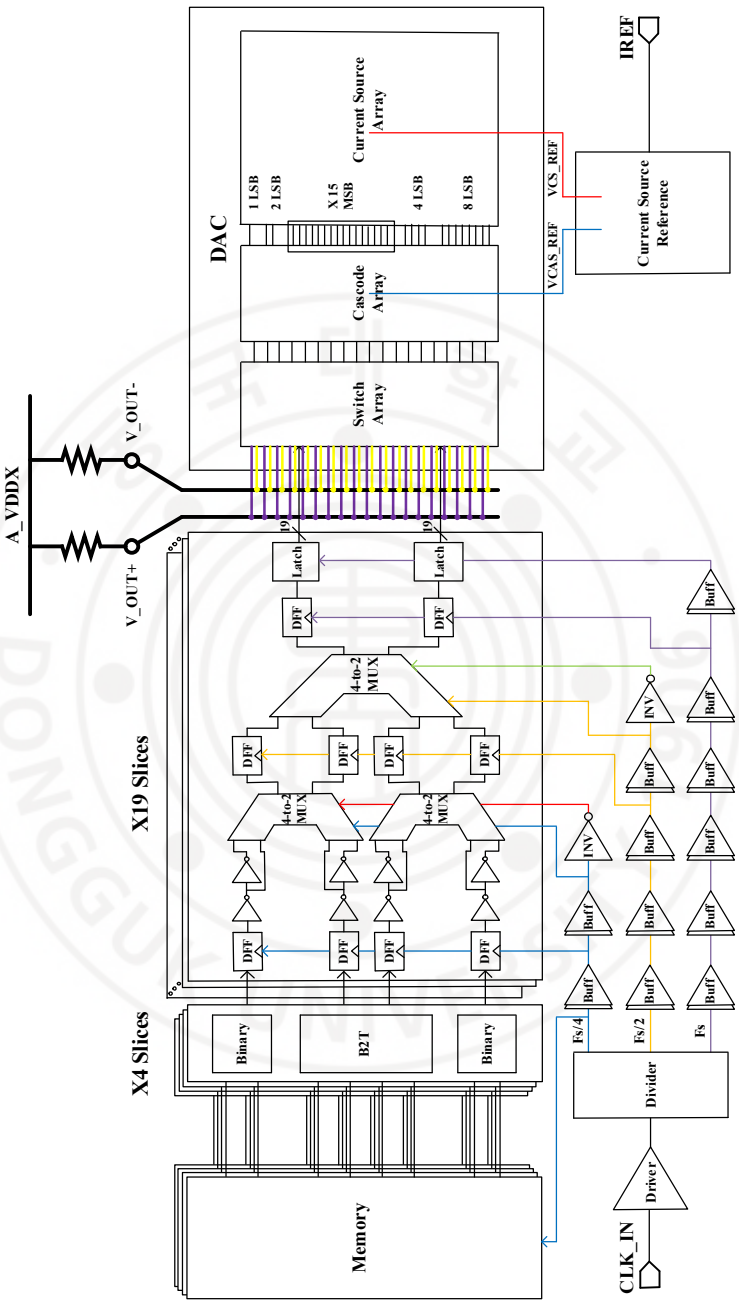

Figure 6.2-1 Block Diagram of Entire 28 nm CS DAC

6.2.2. 40 nm Current Steering RF DAC Architecture

This part contains a description of the 40 nm CS DAC. The design is carried out by supplementing the problems of the previously designed 28 nm CS DAC, and there is a part designed in a different way. Change the existing differential 4 to 2 MUX to single 2 to 1 MUX and use it. The reason is that since the existing MUX has a differential structure, both positive and negative clock trees are needed, and the operation is unstable due to the delay problem. Therefore, single 2 to 1 MUX, which can also reduce the power consumption of the clock tree in half, is used. This also has advantage of the one side layout design of the clock signal. Next, the synchronization circuit part of the connection between the Memory output and the DATA Interface input is further supplemented and designed. Looking at the operation process of the memory mentioned in Chapter 4, it proceeds by stacking sequentially circulating data. However, it is not the sequentially stacked data that the actual CS DAC should receive, but the already stacked sorted data. Of course, the clocks in the memory register part are all designed to fit the same, so the problem of data alignment as it accumulates is solved as a result, but there is a risk. Therefore, the connection between the Memory and the Data Interface is disconnected until the desired data is stacked, and the data is carried out through the switch and the DFF array in a state of being connected from the time when the desired data is stacked. Also, this time, the possibility of calibration is increased by separating the clock in the Memory and the clock in the DATA Interface. And change the existing high

crossing point latch (= switch driver) to high crossing point DFF. This is to further stabilize the data entering the switch of CS DAC, and power consumption is also reduced as the latch stage is replaced by the existing DFF stage. By adding a buffer driven by Analog VDDX between the switch driver and the switch, stable data is sent, and crossing point drop is prevented. Other changes will be explained later.

It is about the delivery of 40 nm CS DAC DATA. This part is similar to the 28 nm CS DAC. First, a total of 128 x 32 (4096) bit of 3 GS/s data are entered into the memory as serial. In this case, when SS is 0, it is a read state, and when SS is 1, it is a write state. The connection to the DATA Interface is disconnected while the 4096 bit data is fully loaded, at which point the differential output of the CS DAC is zero and full scale. When all data is entered and then entered the write state, a total of 32 128 bit 3 GS/s data in circulation are connected to the DATA Interface. Here, first, after data alignment through the DFF array, it enters the decoder. As a result, the output of the decoder sends 76 3 GS/s data and goes through an alignment process through 76 DFF arrays. The sorted data is upconverted to 38 6 GS/s 256 bit data via 38 2 to 1 MUX arrays. Then, the alignment process is performed through 38 DFF array. The rearranged data will go through 38 2 to 1 MUX arrays to use differential pair signals without delay differences. The actual MUX output signal has a delay, but it is matched through the high crossing point DFF of the next stage. Thus, the 38 6 GS/s 256 bit data are upconverted again to 19 differential pair 12 GS/s 512 bit data through 38 2 to 1 MUX array. Next, it is sorted through 38 high crossing point DFF

array, and then data is transferred to the CS DAC through an analog buffer. At this time, the timing between the clock and the data is performed individually because the clock of the memory and the data interface are separated.

It is about 40 nm CS DAC Analog part. The direction of the actual analog part design is the same as the 28 nm CS DAC's analog part design. There are differences in layout and schematic caused by differences in processes. The current source array uses a unique switching scheme that combines Q^2 Random Walk switching scheme and a Hierarchical switching scheme. In addition, a hierarchical switching scheme is applied to the cascode array and the switch array to reduce systematic mismatch. In adjusting the switch parameter, a method different from that of the 28 nm CS DAC is applied, and accordingly, performance is improved. For 50 ohm matching on the output line, matching is done through the CPW line and the actual resistors, and the rest is driven using the 50 ohm microstrip line. Separate each VDDX in the same way as the 28 nm CS DAC. A detailed explanation of the above will be given later.

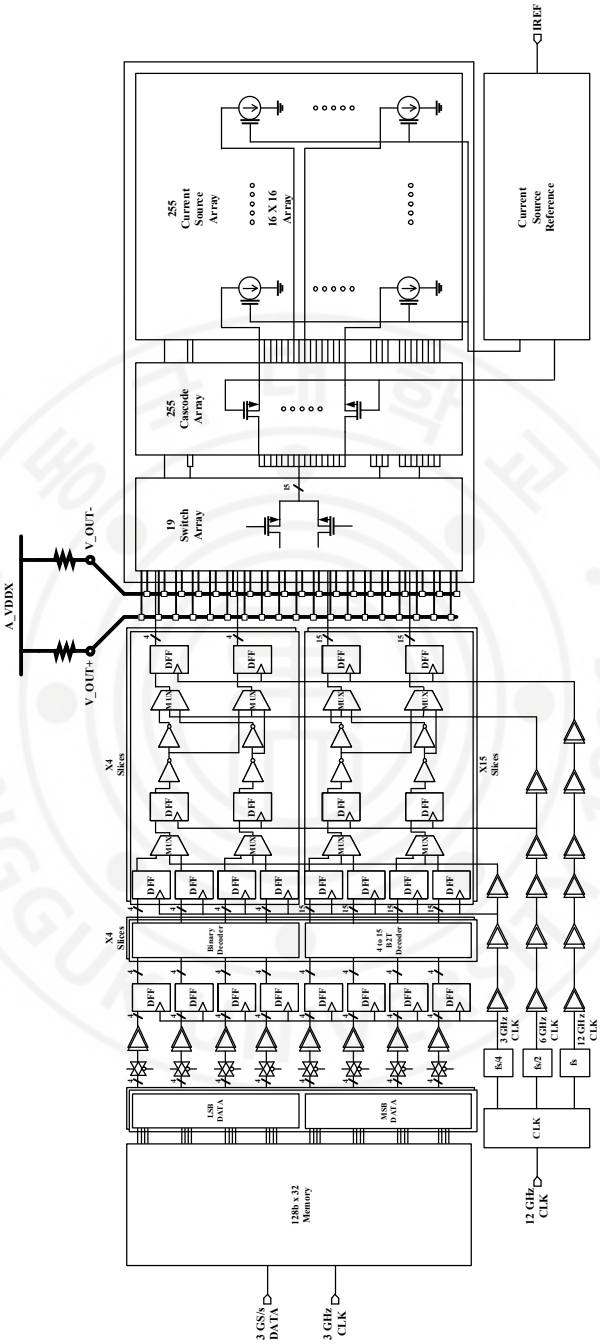

Figure 6.2-2 Block Diagram of Entire 40 nm CS DAC

6.3 Finite Output Impedance Characteristics of Current Steering RF DAC

This is a description of the finite output impedance known as one of the systematic mismatches of the CS DAC. In fact, this finite output impedance is a factor that affects both static and dynamic performance of CS DAC. Looking at the behavior of the CS DAC, we can see how the finite output impedance results in the CS DAC. First of all, the output of CS DAC is a signal that swings from zero scale to full scale voltage according to the full scale current determined by the design. For an ideal CS DAC, for example a thermometer coded CS DAC would flow the same current across all current sources. This means that the drain voltage applied to all current source is constant regardless of the output of the CS DAC. Here, we can see what finite output impedance means. It means that in the actual operation of CS DAC, the drain voltage of the current source changes by layout. The fact that the drain voltage of the current source fluctuates a lot means that the amount of current changes a lot, thus affecting INL and DNL. Therefore, in order to prevent these problems, CS DAC must satisfy high output impedance, which is the same as saying that the change in drain voltage of the current source should be as small as possible. To this end, the practical way to improve is to use a cascode current source and a current source device with a long length. In addition, it is common to operate all devices in the saturation region so that the effect of output voltage acts as little as possible on the drain voltage of the current source. Another important thing to know

is that the current sources of the MSB core and each LSB core in the CS DAC have different drain voltage variations.

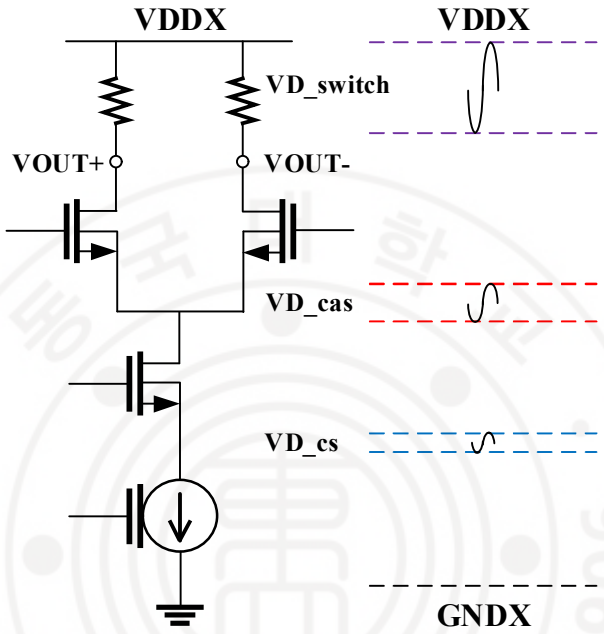

Figure 6.3-1 Simple CS DAC Operation Region

Figure 6.3-1 shows the approximate node voltage operating range of the CS DAC. As mentioned earlier, the CS DAC of this thesis is designed with a 4 MSB and 4 LSB segmented structure. In addition, all cascodes and current sources are composed of unit 1 LSB devices, and in the case of upper LSB and MSB, they are connected by parallel. Therefore, in this CS DAC, only the switch is used as a single device for each individual core. This means that the current flowing through each switch is 1 LSB, 2 LSB, 4 LSB, 8 LSB, and 16 LSB (=MSB), respectively. It can be seen that all drain voltages must be the same for all unit 1 LSB current sources to

flow the same current. However, since the current flowing through each switch is different, the source node voltage of the LSB and MSB switches are different. The assumption at this time is when the parameters of all switch devices are the same. Therefore, additional matching is required, and in this thesis, the parameters of each switch are adjusted. This is possible because when designing, it is designed with margin on all node voltages and satisfies sufficient high impedance. The margin at this time is determined by the overdrive voltage and Vds of the switch in all operating ranges of the CS DAC. Two criteria for adjusting switch parameters will be described later. Figure 6.3-2 shows that the variation of drain voltage is different for each node voltage in the entire CS DAC.

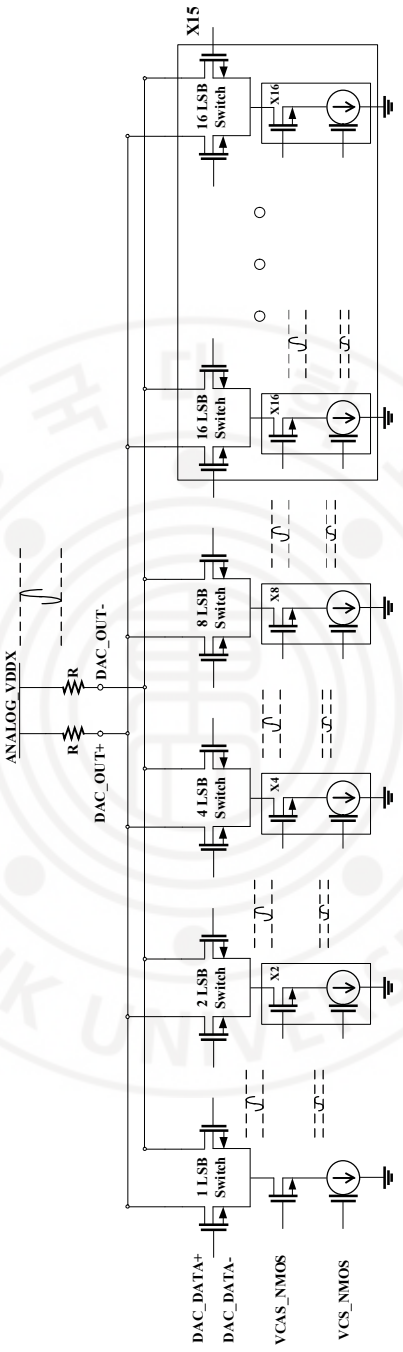

Figure 6.3-2 Current Source Drain Voltage Variation in Entire CS DAC

The 28 nm CS DAC and 40 nm CS DAC are designed with different switch parameter criteria. The reason for this is that the Vth difference between the two CMOS processes allows driving at a high full scale current at 28 nm CS DAC, while driving at a low full scale current at 40 nm CS DAC. Therefore, in the case of a 28 nm CS DAC, the change in the output voltage of the DAC, that is, the drain voltage of the switch, is greater than that of a 40 nm CS DAC. To satisfy the saturation in all digital code sections, the 28 nm CS DAC is conducted in the direction of lowering the source node voltage of the switch, and in this case, a strategy to minimize the current difference is used. It is to equalize the source node voltage of all switches. At this time, of course, all devices satisfy the saturation and set it as a source node voltage with a certain amount of margin. In theory, since all devices under the switch are the same, it can be said that they will all have the same drain voltage. However, there is actually a voltage drop difference due to the length difference of all interconnect lines. In addition, since the degree of swing of the switch source node voltage due to the difference in the switch parameter is all different, it is not possible to have exactly the same current value due to these differences. Nevertheless, by proceeding in this way, it can be confirmed through simulation that performance is improved compared to the existing version. It can be said that the current stability of the current source is the standard for this method.

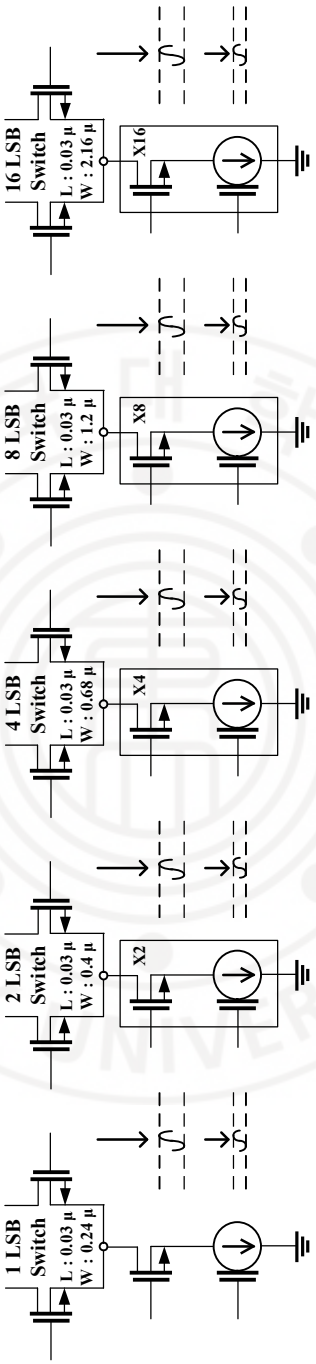

Figure 6.3-3 Switch Parameter for Switch Source Voltage Equalization

The criterion for adjusting the parameter of the switch in the 40 nm CS DAC is different from the existing 28 nm CS DAC criterion. As mentioned earlier, since the full scale current of the 40 nm CS DAC is smaller than the 28 nm CS DAC, the change in drain voltage of the switch is smaller than that of the 28 nm CS DAC. Therefore, there is more margin at switch source node voltage. This time, unlike before, the switch source node voltage is increased, and in this case, a strategy is used to minimize the capacitance of the switch by reducing the Vds of the switch. In this case, the upper limit criterion of the switch source voltage is based on the crossing point of the switch data and that all devices satisfy the saturation at the same time. The explanation of this will be given in the next part. This time, the source node voltage of each switch is not the same because the data crossing point is the standard. However, due to the long length current source (=high output impedance), the current flowing through each current source has little difference. At this time, there is a difference in gain from the standard CS DAC. The biggest advantage of proceeding in this direction is that the settling time of the switch is lowered. In addition, because the drain voltage of the cascode and current source has an additional margin than the existing CS DAC, it is possible to operate more stably. It can be confirmed through simulation that this method also improves performance compared to the existing version. In this method, it can be said that the minimum capacitance of the switch and the additional margin of the devices below the switch are the criteria.

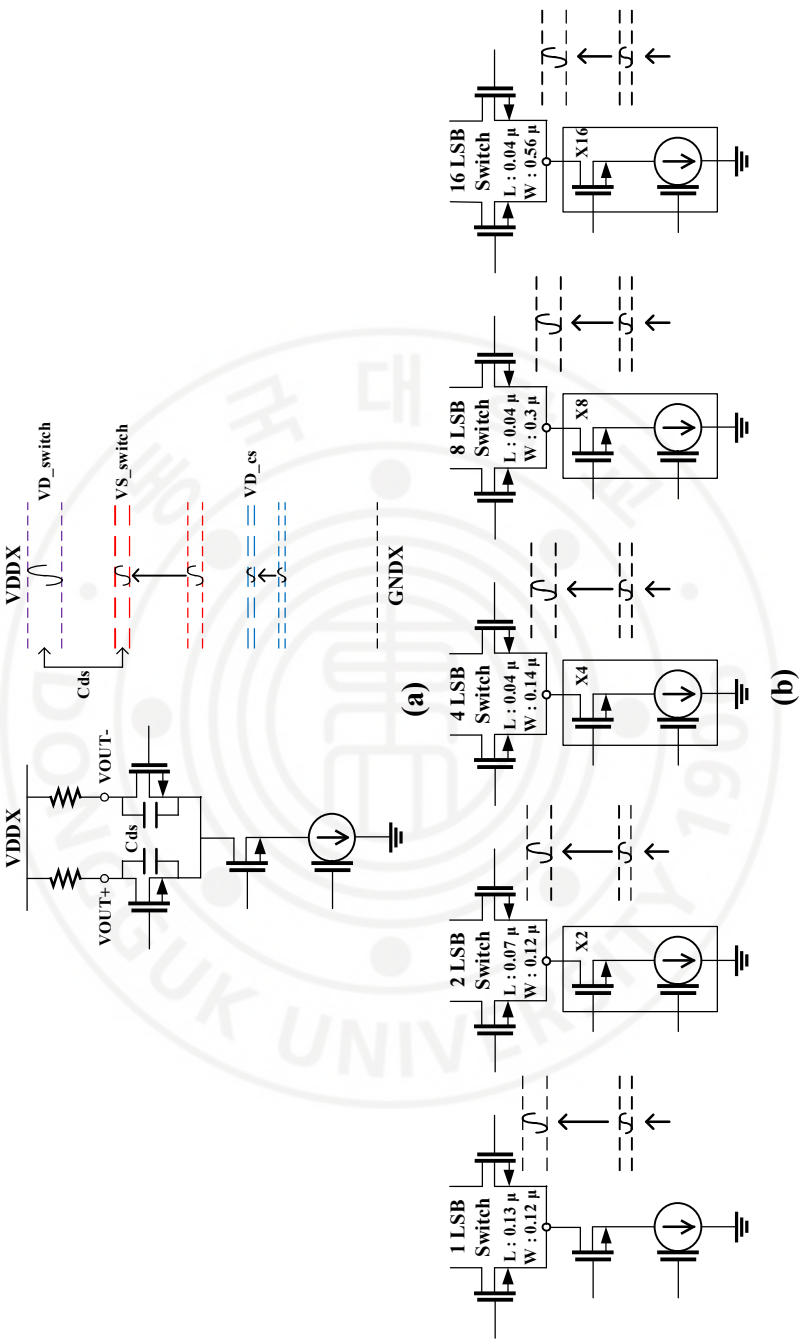

Figure 6.3-4 (a) Switch Capacitance Minimization Concept (b) Switch Parameter for Switch Capacitance Minimization

As can be seen from the previous contents, the finite output impedance problem of CS DAC is a problem that cannot be completely solved. Therefore, in this thesis, the performance of CS DAC is improved by using the above two concepts. This can also be said to be a method using the high output impedance of CS DAC. This part describes exactly what is caused by the finite output impedance of the CS DAC. The operation of the CS DAC, which can best check this part, can be confirmed in the 1 LSB digital code shift operation to check INL and DNL. This is also related to the code dependent error mentioned in other papers. In other words, it has a similar meaning, such as finite output impedance and code dependent error. Finite output impedance generally means that the drain voltage of the current source varies depending on the output of the CS DAC. In general, code dependent error means that the switching transient is changed according to the change in code, which has a bad effect. As a result, this means that the number and location of switches switched according to the change in output of CS DAC are all different, and this also comes from the change in node voltage of switch, cascode, and current source by CS DAC output voltage, so it has a similar meaning to finite output impedance. In fact, in order to understand these principles, it is the most accurate way to see the behavior of CS DAC.

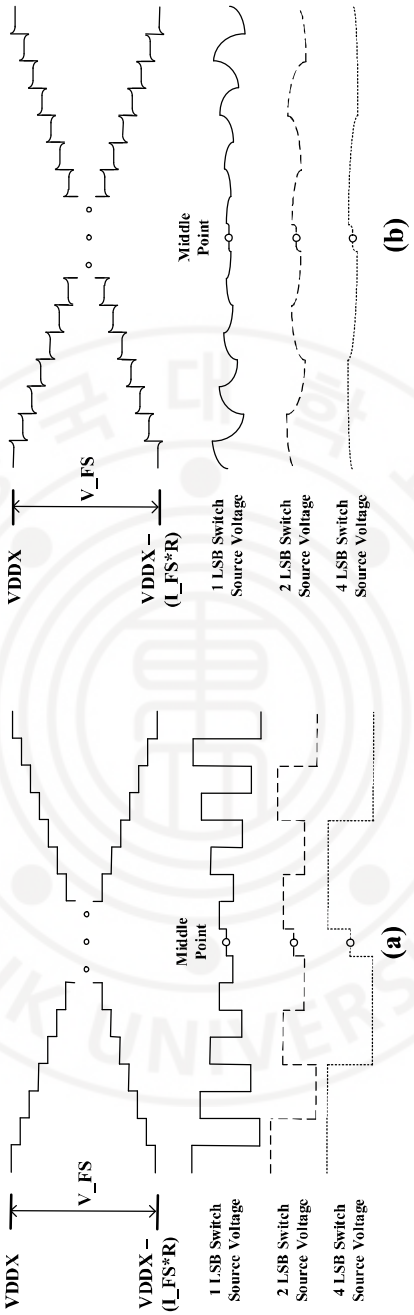

Figure 6.3-5 Simple CS DAC 1 LSB Digital Code Shift Operation (a) at Low Frequency (b) at High Frequency

Figure 6.3-5 gives a rough idea of what CS DAC's finite output impedance is actually like. One thing to note here is the difference that appears during high frequency operation. Unlike low frequency operations, when operating at high frequencies, the capacitance of devices affects the actual operation. Therefore, dynamic elements such as glitch are added in a switching transient situation. However, a significant point is the swing of the switch source voltage. The node voltage of each switch is changed for each digital code. The steady state is sufficient for the low frequency operation, but the swing is large, while the high frequency operation lacks the steady state and the swing is small. This point is a response determined by the capacitance and resistance of devices, so it is difficult to find improvements. However, the small swing of the switch source voltage means that the swing of the drain voltage of the current source is also small, so if all devices satisfy the saturation region in all sections, the current difference will not be large. In addition, the code dependent error varies depending on the degree of switching capacitance between the switch source and drain voltage according to the change in code. It is possible to minimize the Vds voltage difference through the criteria applied to the 40 nm CS DAC. It can also be seen from this that the full scale current of the CS DAC itself is directly involved in the code dependent error.

6.4 DATA Crossing Point Characteristics of Current Steering RF DAC

It contains a description of the data crossing point of the current steering RF DAC. This part is about adjusting the crossing point to prevent the simultaneously turn off switch in Chapter 3. The contents of the crossing point in the existing CS DAC papers simply focus on the high crossing point itself, which prevents the switch from turning off at the same time. Therefore, it does not explain to what extent this high crossing point should be raised or what additional considerations arise. As mentioned earlier, in a crossing point situation where the switch is turned off at the same time, the source node voltage of the switch is charged again after being discharged. Therefore, it takes time to charge again, and because the drain voltage of the current source is also discharged due to switch source node voltage discharge, glitch occurs. This has a nonlinear effect on CS DAC. The data of the high crossing point, which is this solution, also changes the source node voltage of the switch. In this case, it is operated in the form of distribution rather than the concept of discharge and charge, and the existing current is distributed to the differential switch. Therefore, the source node voltage of the switch increases because the existing current must be distributed in a situation where the gate voltage of the switch is lower than the target voltage. As a result, it can be seen that the current does not change rapidly in the case of a simultaneously turn on situation, so the linearity of the current source increases rather than in the simultaneously turn off situation. The primary criterion of the

crossing point is to hold the crossing point higher than the turn on voltage of the switch while all devices satisfy the saturation region.

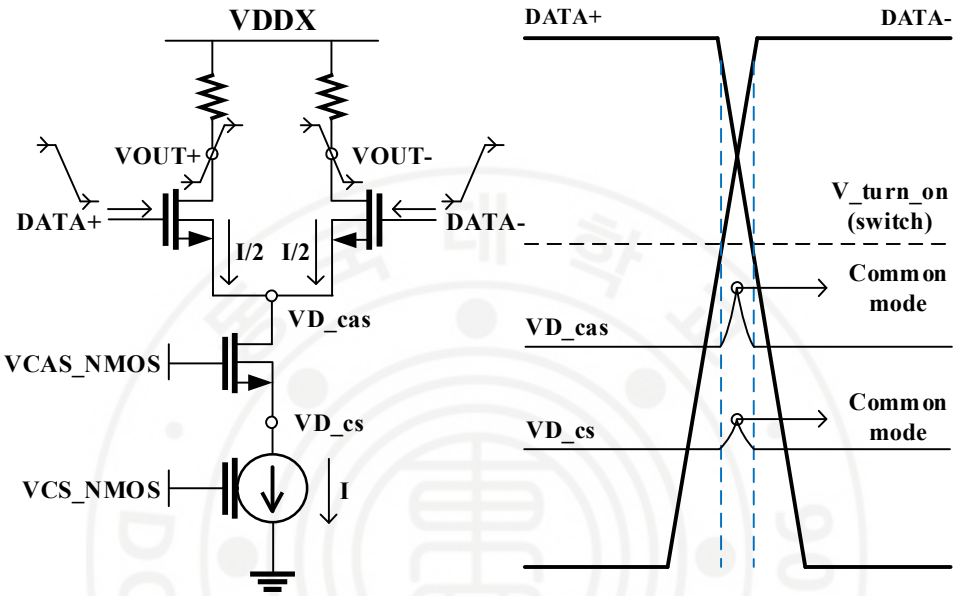

Figure 6.4-1 Simultaneously Turn On Switch Concept

The above figure shows the contents of the high crossing point concept applied to the 28 nm CS DAC. For a 28 nm CS DAC, since the full scale current is 4 mA, there is a 200 mV swing in the drain voltage of the switch. Therefore, in order to satisfy the saturation of the switch, the switch source node voltage of all CS DAC cores must must be lowered, so the switch source node voltage of all CS DAC cores is designed to be the same and to give high crossing point date. As can be seen from the Figure 6.4-1, at the crossing point, differential switches are turned on at the same time, and thus, half of the current flows by the common mode operation.

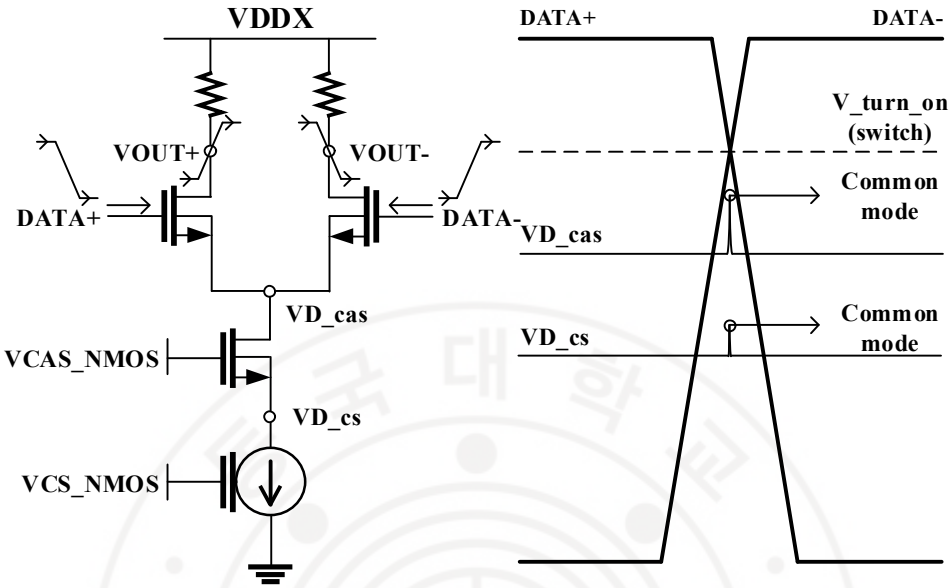

Figure 6.4-2 High Crossing Point Optimization Concept

The above figure shows the contents of the high crossing point optimization concept applied to the 40 nm CS DAC. Unlike the 28 nm CS DAC, the 40 nm CS DAC has a full scale current of 1 mA, with a 50 mV swing at the drain voltage of the switch. Therefore, the voltage headroom problem of the source node voltage of the switch is less than that of the 28 nm CS DAC. The high crossing point concept mentioned in existing papers has no clear standard. Therefore, although there will be various reference points in practice, one of them is described as a clear reference point. The basic concept is to fit the turn on voltage of all core switches in the CS DAC to the crossing point. In fact, the reason why this method is possible is that the current source has sufficient impedance. The advantage of this is that the switching section of the switch is significantly reduced, and thus the settling time is reduced.

In addition, since the source node voltage of the switch is raised to meet this criterion, the difference in drain source voltage of the switch is reduced. Therefore, as the device capacitance of the switch decreases, there is an additional advantage in terms of settling time and glitch.

6.5 Circuit Implementation

This is a description of the current steering DAC designed at 28 nm and 40 nm. Since there is already an explanation of the overall structure and each parameter of CS DAC, new changes and additional design methods will be explained here. A basic CS DAC designed at 28 nm and 40 nm uses a DNW device, unlike a 28 nm TI DAC. DNW device is designed by customizing it. The figure below shows the parameters and layout of each device used in the 40 nm CS DAC. Switch device shows only parameters of 1 LSB switch.

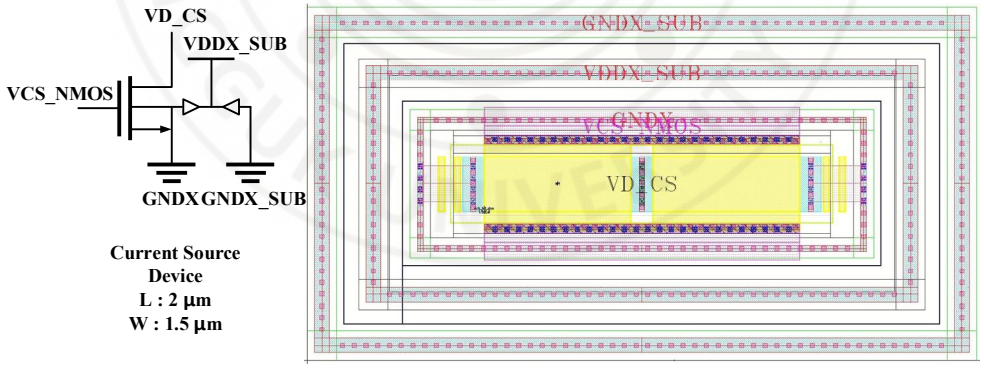

Figure 6.5-1 Current Source DNW Device Parameter & Layout

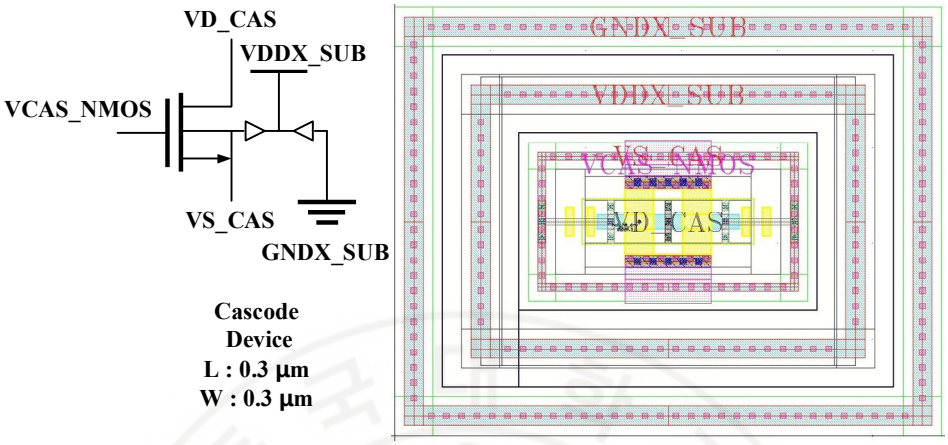

Figure 6.5-2 Cascode DNW Device Parameter & Layout

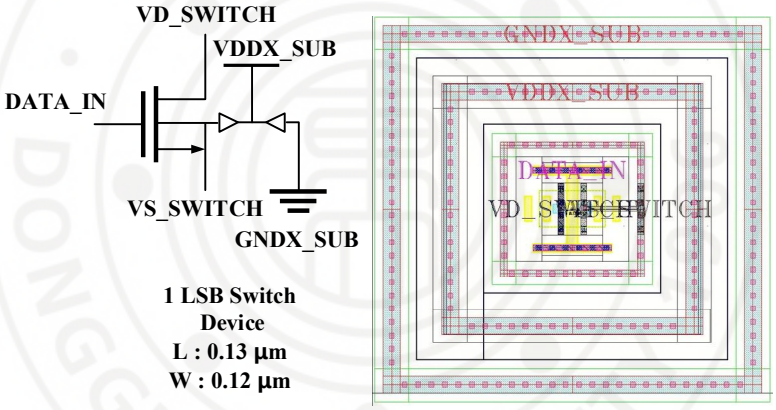

Figure 6.5-3 1 LSB Switch DNW Device Parameter & Layout

Next, the newly changed part is the switching scheme part of the current source array. The before TI DAC applies Q^2 random walk switching scheme to the current source array and a hierarchical switching scheme to the cascode and switch array above. This design uses a scheme that combines the above two switching schemes for the current source array. In addition, a hierarchical switching scheme is applied simultaneously to the cascode and switch array above. Unlike TI DAC, this basic CS

DAC uses 4 to 1 data interleaving. Therefore, as the number of cells in the data interface increases, the additional delay difference in the decoder part is more severe than before. Therefore, the hierarchical switching scheme is used in the order in which this delay can be alleviated a little more. On the layout design, the GNDX line is not only supplied with UTM but also more stable GNDX through additional connection between the metals below. In addition, the same GNDX line above and below the current source signal line and the same metal line are used to minimize mismatch, but perfect compensation of the length difference of the line is impossible. The Figure 6.5-4 shows the actual switching scheme and the alignment order.

As the DNW device is used, there is a limitation in layout design. Due to the metal required for additional VDDX line connection due to the use of DNW and additional metal lines for more stable GNDX, the available metal is less than before. Also due to the larger size and DNW's drc rule, a tight design is impossible. Therefore, even if the area is slightly increased, the layout design is a s symmetric as possible, the design that can match the area of the cell in the data interface one to one, and the influence between current lines in different directions is as small as possible. Figure 6.5-5 shows the actual line connection of 1 MSB core.

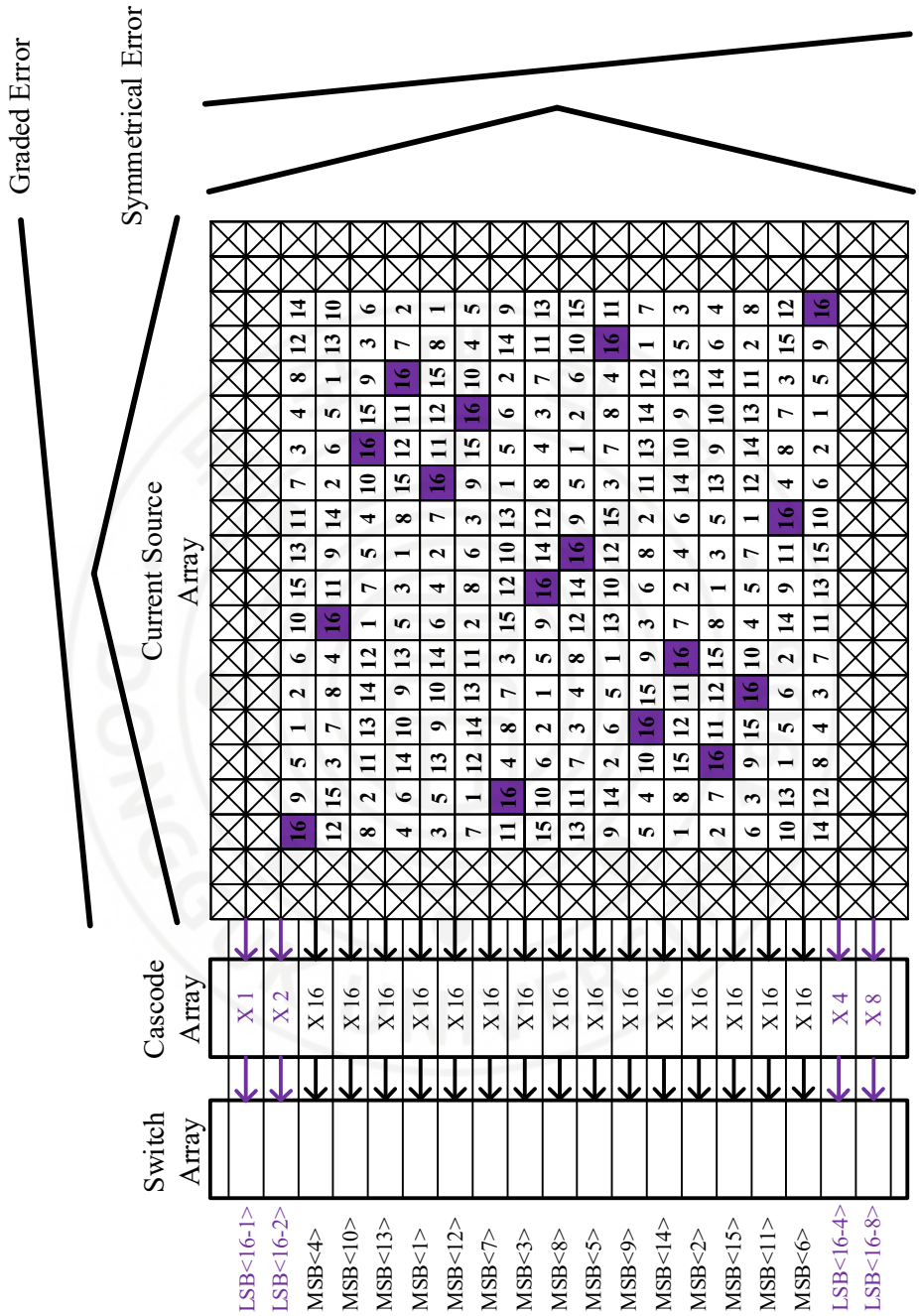

Figure 6.5-4 Custom Switching Scheme

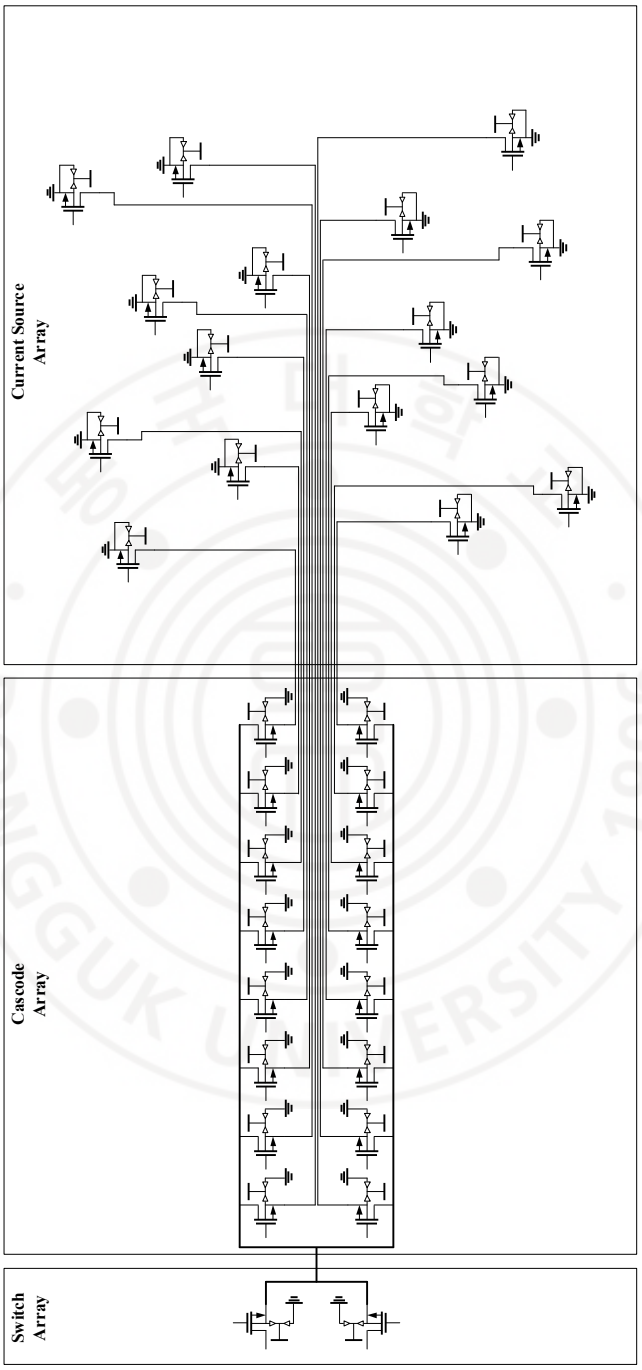

Figure 6.5-5 1 MSB Core Interconnect Connection Method

6.6 Simulation Results & Measurement Setup

It contains information on simulation results and measurement setup of 28 nm and 40 nm CS DACs. First of all, the figure below shows the result of digital code 1 LSB shift post layout simulation of 28 nm CS DAC. At this time, the sampling rate is 16 GS/s, and the swing of 200 mV from 1 V to 0.8 V can be checked according to the full scale current of 4 mA.

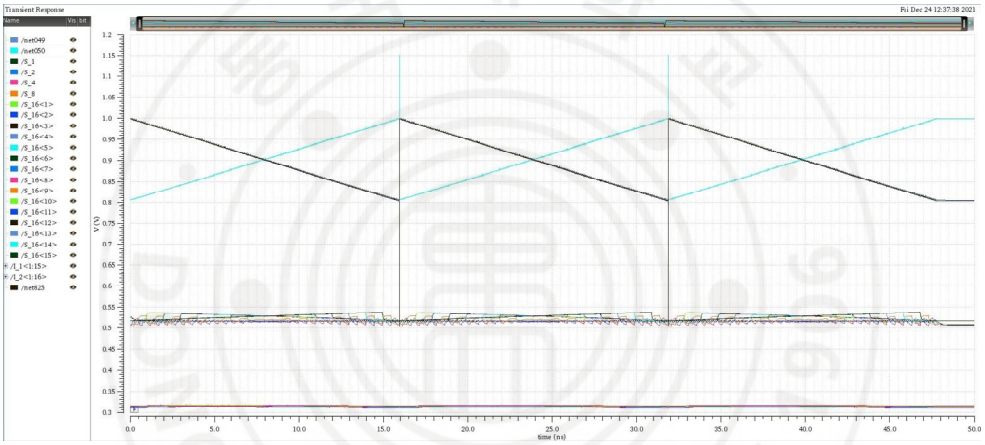

Figure 6.6-1 28 nm CS DAC Digital Code 1 LSB Shift Post Layout Simulation Result

The following figure shows a 28 nm CS DAC chip and layout. Currently, wire bonding and PCB production have been completed, and measurement is currently scheduled. The size of the 28 nm CS DAC chip is 1.8 mm x 1 mm.

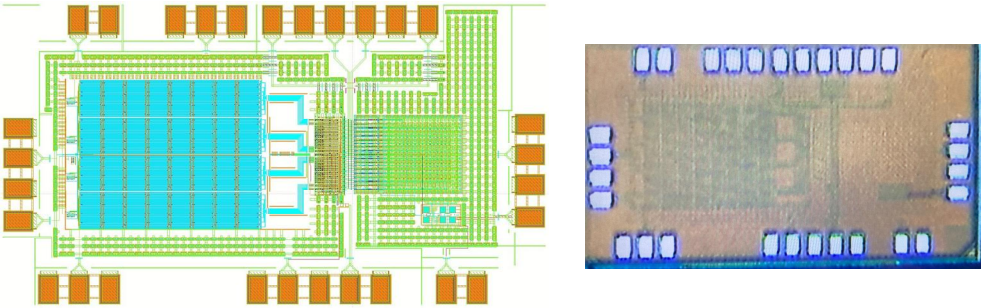

Figure 6.6-2 28 nm CS DAC Layout and Chip

The figure below is about the measurement setup of the 28 nm CS DAC. The input of the memory is made using cheetah, and the rest of the signals except 16 GHz clock and DAC output are entered through PCB and wire bonding.

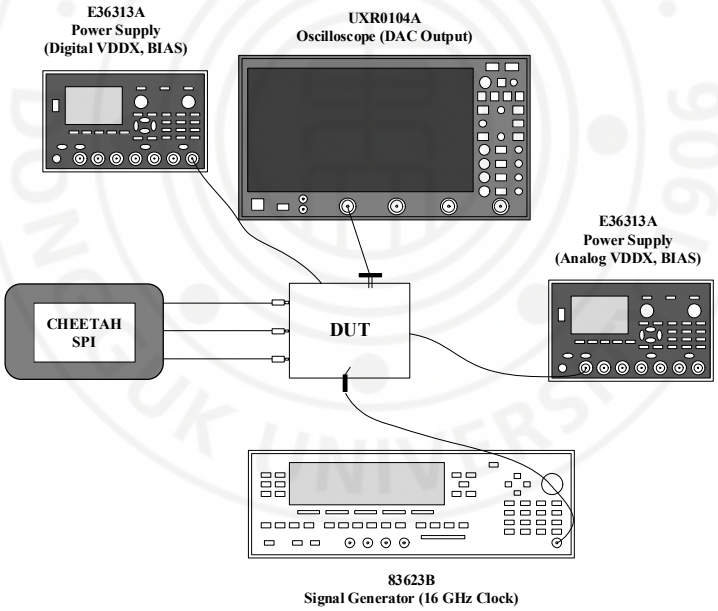

Figure 6.6-3 28 nm CS DAC Measurement Setup

Next, it is about simulation results and measurement setup of 40 nm CS DAC. The figure below shows the result of digital code 1 LSB shift post layout simulation

of 40 nm CS DAC. In this case, the sampling rate of CS DAC is 12 GS/s. It is possible to confirm a swing of 50 mV from 1.1 V to 1.05 V in accordance with 1 mA, which is the full scale current of CS DAC.

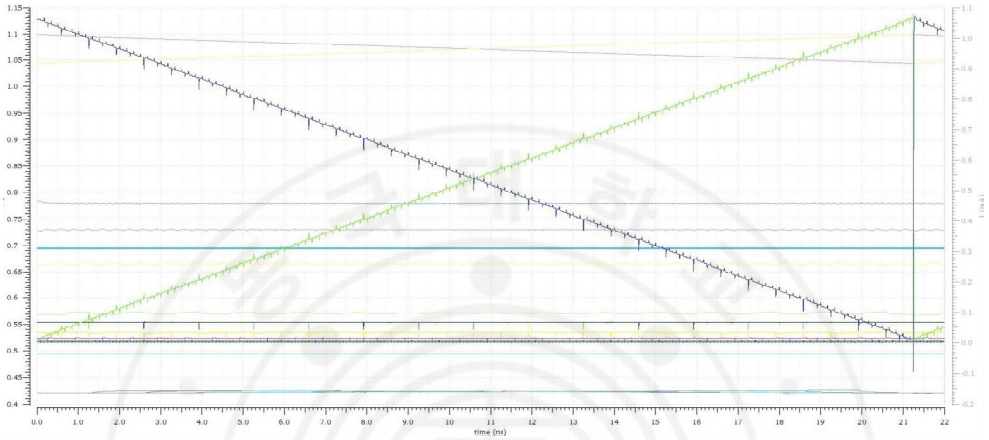

Figure 6.6-4 40 nm CS DAC Digital Code 1 LSB Shift Post Layout Simulation Result

The following is the result of 40 nm CS DAC SFDR simulation. It is confirmed through cadence spectrum simulation, and is the SFDR result of the Nyquist frequency situation. It shows SFDR performance of about 75.8 dBc.

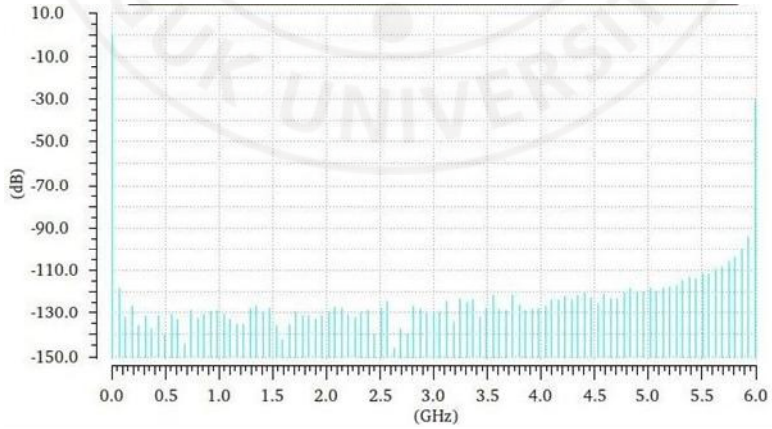

Figure 6.6-5 40 nm CS DAC SFDR Simulation Result at Nyquist Frequency

Next is a picture of the entire chip layout of the 40 nm CS DAC. The size of the 40 nm CS DAC chip is 1.5 mm x 1 mm.

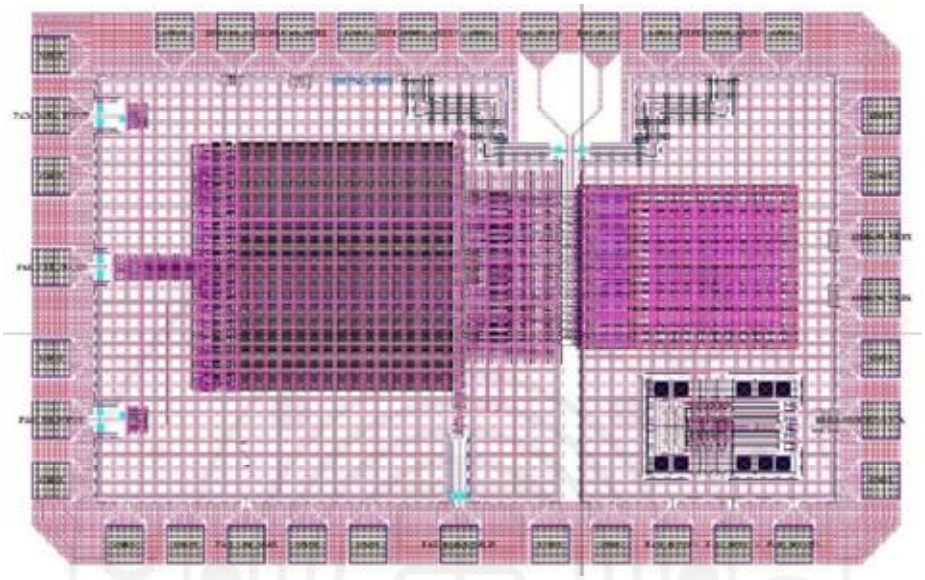

Figure 6.6-6 40 nm CS DAC Layout

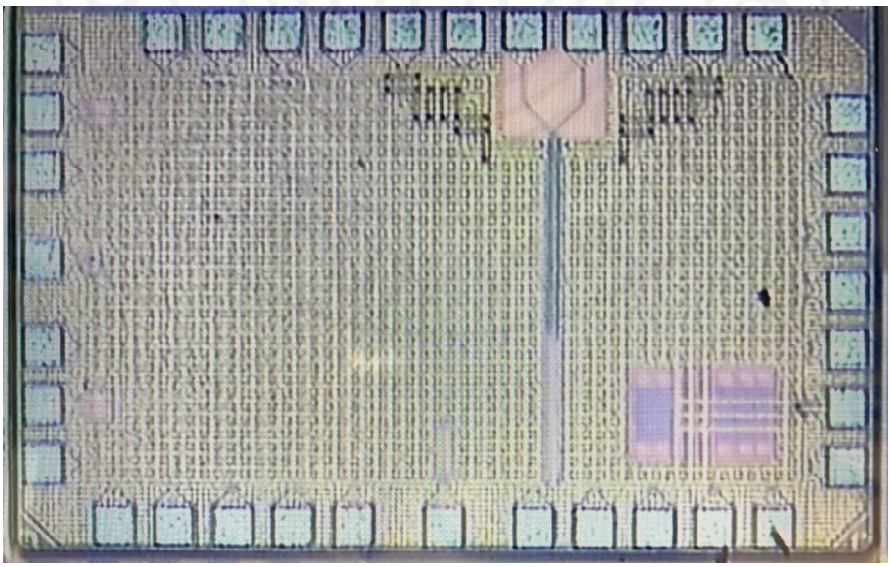

Figure 6.6-7 40 nm CS DAC Chip

Finally, measurement setup of 40 nm CS DAC. Unlike the existing CS DAC, the clock is used separately, so two signal generators are required. At this time, data entering the memory and SS receive information from the AWG to the SMA connector through PCB and wire bonding. Next, in the case of clock signals, 3 GHz and 12 GHz clocks are supplied as probe tips through two signal generators. The output of the CS DAC is connected to the oscilloscope through a probe tip, and the remaining signals supply DC and bias using PCB and wire bonding.

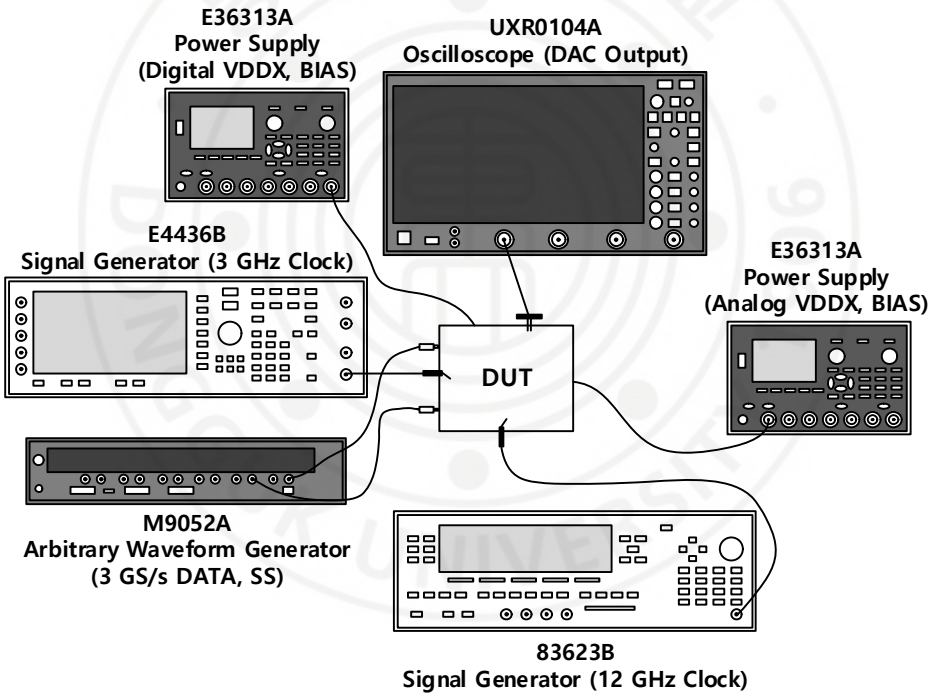

Figure 6.6-8 40 nm CS DAC Measurement Setup

Chapter 7 Conclusions

By approaching and applying it from a different point of view from the existing

method, the performance of the CS DAC is improved, and the performance is better than that of the DACs of other papers. Also, by suggesting a new method, it can be seen that there is still a lot of potential for the development of not only CS DAC but also TI CS DAC.

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국문 초록

본 학위 논문은 직접 디지털 파형 합성에 필요한 초고주파 대역 8 bit 전류 조절 디지털 아날로그 변환 회로를 제안한다. 기존의 수퍼 헤테로다인 송신기 방식과는 다르게 직접 디지털 파형 합성 방식은 복잡한 합성, 필터 사용 방식을 초고주파 대역 디지털 아날로그 변환 회로로 대체하는 편리함을 가지며, 이에 따라 DAC는 높은 기본 신호 대 스퓨리어스 신호비(SFDR) 성능을 필요로 한다. 높은 집적도를 위한 CMOS 기술을 사용했으며, 2중 채널 및 단일 채널 방식의 DAC를 제작했다. 2중 채널 DAC의 샘플링 속도는 4 GS/s 이며, 단일 채널 DAC의 샘플링 속도는 각각 12 GS/s, 16 GS/s 이다. 면적 문제로 인해 2중 채널 DAC는 twill-well NMOS로, 단일 채널 DAC는 triple-well NMOS로 설계했다. 구현된 단일 채널 12 GS/s DAC에서는 post layout simulation을 통해 Nyquist frequency(6 GHz)에서 8 bit 유효 비트 수(ENOB), 69.4 dB 신호 대 잡음비(SNR), 75.8 dBc 기본 신호 대 스퓨리어스 신호비(SFDR) 특성을 갖는다.