Thesis for the Degree of Master of Engineering

Studies of Low Dropout Regulators for Analog and Digital Systems in CMOS Technology

Advisor: Professor Jung-Dong Park

Graduate School of Dongguk University
Department of Electronic and Electrical Engineering

Junhee Lee

2023

Thesis for the Degree of Master of Engineering

Studies of Low Dropout Regulators for Analog and Digital Systems in CMOS Technology

by

Junhee Lee

Advisor: Professor Jung-Dong Park

Date of submission : 2022/12

Date of approval : 2023/01

Approved by:

Chairman : Professor Sangjin Byun (Sign)

Committee member : Professor Minsung Kim (Sign)

Committee member : Professor Jung-Dong Park (Sign)

Graduate School of Dongguk University

ACKNOWLEDGEMENTS

Before starting my thesis, I would like to express my gratitude. Professor Jung-Dong Park has guided me through my master's course. He had gave me clear and prompt advice, was kind, and full of insight. He gave me sincere advice both in research and personal life. He inspired me to cerebrate new ideas and was always open to them. He also took care of future career of every students in the lab. I would not have completed my master's course without his guidance.

I always relied on Jeong-Moon Song, our laboratory chief, whenever I had difficulties with research. He helped me a lot with kindness. Laboratory alumni Dr. Hyohyun Nam, Dr. Van-Son Trinh, Young-Joe Choe, Hsiang Nerng Chen, Hyeonseok Lee gave me many advices. All the lab members including Tae-Hwa Hong, Hyeong-Geun Park, Le Van Du, Nguyen Van Phu, and Jun Kwon voluntarily helped each other and evolved.

Last but not least, I want to thank my family, friends, and my lover. They gave me much support throughout the whole course, and sacrificed themselves to let me immerse myself in research.

Junhee Lee

ABSTRACT

This thesis proposes Flipped Voltage Follower(FVF) Low-Dropout Regulator(LDO) for analog systems and Ring LDO for digital systems. Dual-loop FVF LDO is designed and fabricated in TSMC 65nm CMOS technology to meet the specifications needed for analog systems. Proposed FVF LDO consists of slow loop for high Power Source Rejection (PSR) at low frequency and fast loop for PSR at high frequency, which results in PSR across wide frequency range. Fast loop includes super source follower to drive pass transistor and enhance loop operation speed while consuming less power. State matrix decomposition method is employed to analyze the stability of multiloop LDO with parameter variation. The implemented FVF LDO achieved line regulation of 1.04uV/mV within an input voltage range of 1.2V-1.6V, unity gain frequency of 469 MHz, 66dB of low frequency PSRR and was stable within output current range of 2mA-20mA. Ring LDO is designed and fabricated in Samsung 28nm CMOS technology to meet the specifications needed for digital systems. Dynamic bias cascode ring amplifier is used to reduce quiescent current and maintain response time. The cascode amplifier enhances closed-loop gain and PSRR is significantly improved compared to digital LDOs. Implemented Ring LDO has an input voltage range of 0.4V-1.2V, output current density of 55000 mA/um2, and worst-case settling time of 28ns when load current step from 2mA to 20mA. The Ring LDO employs scalable ring amplifier, making it suitable for fully-

integrated LDO for digital systems and occupy small active area since it comprises simple logic gates and capacitors.

TABLE OF CONTENTS

List of Figures

List of Tables

Chapter 1 Introduction

1.1 Research background

With rapid growth of portable device and low-power IoT(Internet-of-Things) equipment, Power management is one of main concern for electronics. In battery operated devices such as biosensor and mobile processor where supply voltage constantly varies, Power management circuit should ensure constant supply voltage with high efficiency. Switching regulator can be one of the options because of high power efficiency it can achieve. However, constant ripple in output and electromagnetic interference (EMI) from switching operation can impact circuit performance. Moreover, switching regulator typically need bulky off-chip inductor which increases overall cost compared to monolithic implementation. Linear regulators are known for lower power efficiency, but linear regulators offer clean output with less ripple and noise.

In this thesis, design considerations for each analog and digital systems are investigated. Flipped voltage follower (FVF) based analog LDO with full-spectrum power source rejection and good low-frequency PSR is proposed for analog circuit systems. Ring LDO with dynamic bias cascode ring amplifier is also proposed. The ring LDO can be implemented in scaled technologies while not sacrificing PSR and transient response. Dynamic bias cascode ring amplifier can reduce quiescent current and maintain transient response time.

1.2 Thesis Organization

In Chapter 2, basic operation principle of LDO is explained. Performance metrics to evaluate static and dynamic performance of LDO is also introduced. Then, key design objective of LDO for analog and digital electronics is discussed. In Chapter 3, FVF LDO for analog circuit is proposed. PSR and stability of FVF LDO is analyzed and simulated. State matrix decomposition[1] is applied to evaluate stability of LDO across parameter variation without breaking the loop. Measurement setting and result are also shown. In Chapter 4, Ring LDO with dynamic bias cascode ring amplifier is presented. Ring amplifier for scalable analog amplification in nanoscale CMOS technology is also explained. Simulation result of PSR and transient response is included. Chapter 5 concludes this thesis and suggests future research.

Chapter 2 Low-Dropout Regulator (LDO)

2.1 Low-dropout regulator

Linear regulator regulates output voltage by modulating series resistance. Voltage drop across series element is controlled such that output voltage is constant. Figure 2.1-1 shows schematic diagram of linear regulator. Series element R_{PASS}, control circuit, and load R_L, C_L is shown.

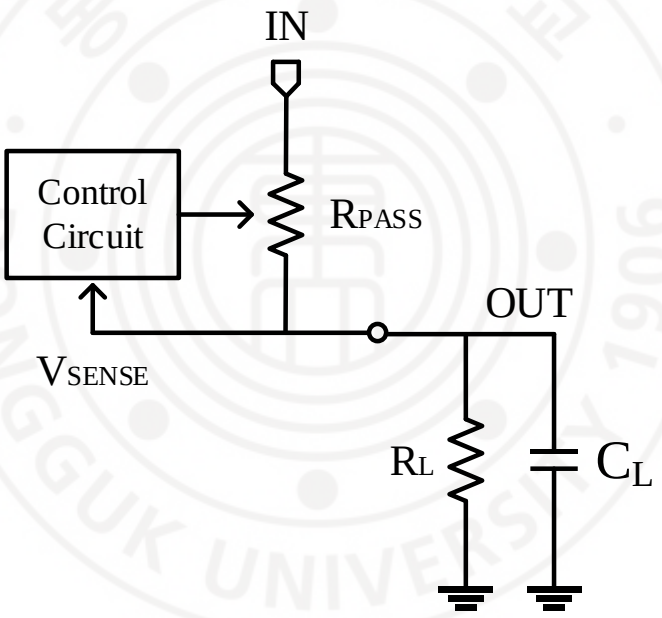
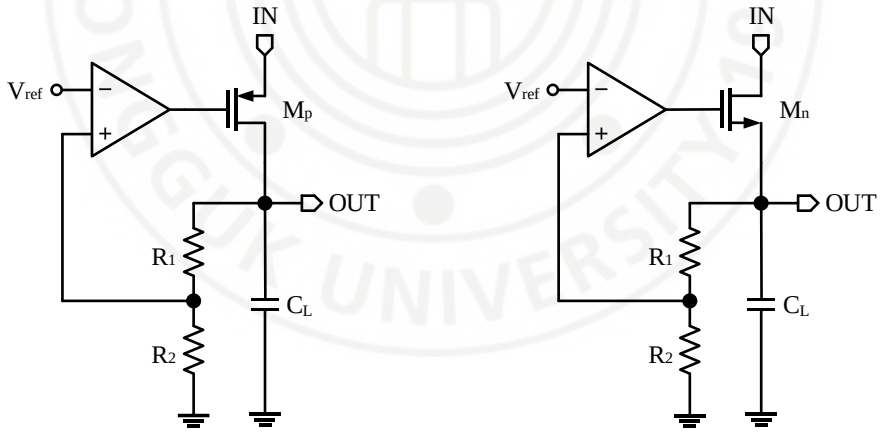


Figure 2.1-1 Linear regulator.

Low dropout regulator includes transistor for pass element and control circuit controls gate voltage of pass transistor. Figure 2.1-1 shows PMOS LDO and NMOS LDO. Error amplifier senses output voltage and control the pass element accordingly. PMOS LDO employs PMOS transistor as pass element and NMOS LDO employs

NMOS as pass element. PMOS and NMOS yields opposite polarity of process gain, so error amplifier input polarity should be opposite in order to form negative feedback. The drain of PMOS transistor is connected to output of PMOS LDO and the source of NMOS transistor is connected to output of NMOS LDO. This makes dominant pole design of each LDO different, since resistance seen at output node is much lower at NMOS LDO than PMOS LDO. In order to turn pass transistor on, gate voltage of NMOS LDO should be at least higher than output voltage by Vth. Gate voltage often become higher than input voltage V_{IN} in NMOS LDO. Therefore the error amplifier should be supplied with higher V_{DD}, or additional techniques such as charge pump is needed. On the other hand, the gate voltage of PMOS LDO should be lower than V_{IN}, so no additional components are needed.



(a) (b)

Figure 2.1-2 (a)PMOS LDO and (b)NMOS LDO.

Next, performance metrics of LDO are explained. Dropout voltage, line regulation, load regulation, and quiescent current are static performances of LDO. Power source rejection ratio, line transient response, and load transient response are dynamic performances of LDO.

2.1.1 Static performance

Ideal LDO should output constant voltage regardless of supply voltage or load current. However, real LDOs have regulation region in which voltage regulation actually works. The voltage drop across pass transistor for minimum supply voltage within regulation region is dropout voltage. The rate of change of output voltage with respect to input voltage is line regulation. Figure 2.1-3 illustrates this point.

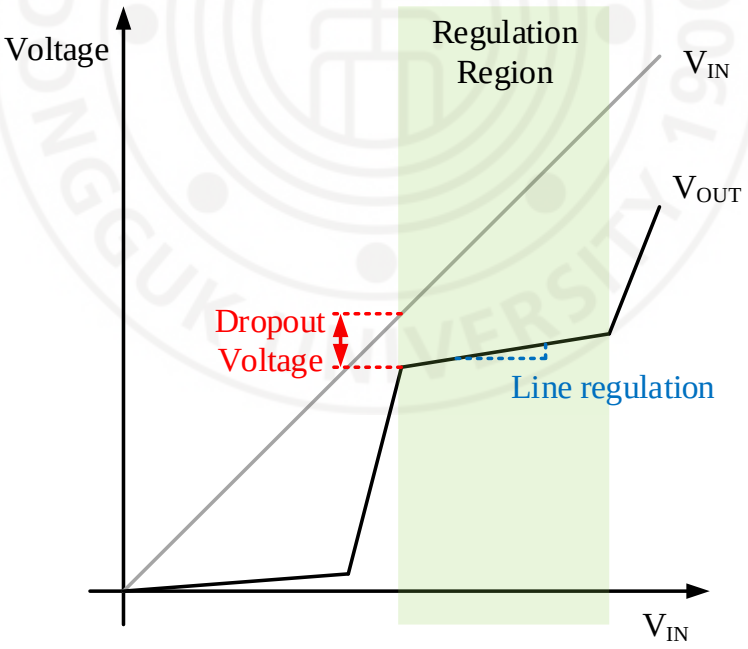


Figure 2.1-3 Typical LDO Output voltage versus input voltage.

The rate of change of output voltage with respect to output current is load regulation. Load regulation is also small-signal output resistance seen at output. The current consumption of internal circuitry of LDO is quiescent current. Low quiescent current is essential for current efficiency of LDO.

2.1.2 Dynamic performance

Power source rejection ratio(PSRR) represents the capability of LDO to reject the ripple or noise/interference from input. PSRR is given by

$$\text{PSRR [dB]}=20\log_{10}\frac{v_{\text{out,ripple}}}{v_{\text{in,ripple}}} \tag{2.1-1}$$

where $v_{\text{in,ripple}}$ is input ripple amplitude and $v_{\text{out,ripple}}$ is output ripple amplitude.

Line transient response is how the LDO responses to supply voltage step. Figure 2.1-4 illustrates typical line transient response of LDO. t_{SETTLE} is time taken for LDO to settle to final output. Transient line regulation is

$$\text{Tran. line reg.} = \frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} \tag{2.1-2}.$$

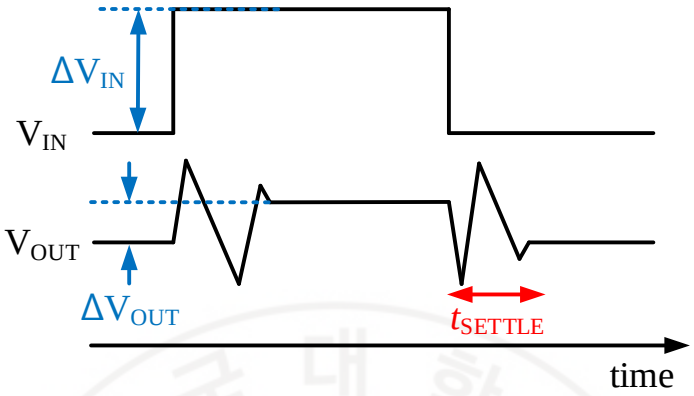


Figure 2.1-4 Typical Line transient response of LDO.

Load transient response represents how a LDO responds to transient load current step. Figure 2.1-5 illustrates typical load transient response of LDO. t_{SETTLE} is time taken for LDO to settle to final output. Transient load regulation is

$$\text{Tran. load reg.} = \frac{\Delta V_{out}}{\Delta I_L} \quad (2.1\text{-}3).$$

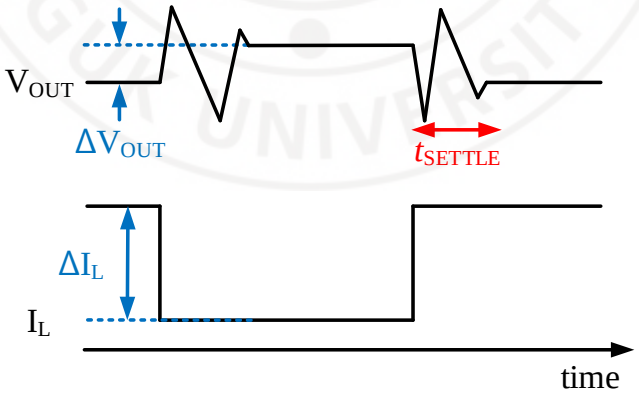


Figure 2.1-5 Typical load transient response of LDO.

2.2 LDO Design objective

Power management system often incorporates switching regulator along with LDO. The switching regulator first regulate the supply voltage close to circuit operation voltage to ensure power efficiency, and the LDO rejects supply ripple coming from switching regulator. Designer should design the LDO to meet various system requirements. Output voltage variation with load current or supply voltage can induce circuit performance variation. Adequate line/load regulation of LDO is needed to ensure circuit performance. Excess dropout voltage can impact power efficiency of power management system. Quiescent current should be minimized in order to ensure current efficiency. Dynamic performance of LDO should also be optimized. Main design objective of dynamic performance varies according to the type of the system, whether the system is analog or digital.

2.2.1 LDO for analog systems

For analog systems such as automotive radar, mobile communication, and bio signal sensors, Sensitive circuit blocks like PLL, ADC, mixers are widely adopted. LDO should reject supply ripple or interference from other components. To ensure the proper operation, the power management circuit must supply stable and isolated supply voltages to each sensitive block, such as the PLL, mixer, and ADC[2]-[11]. Figure 2.2-1 exemplify such situation. Not only control voltage V_{cont} controls output frequency of voltage controlled oscillator (VCO), but the supply voltage can also change the frequency. Moreover, Power supply ripple frequency is modulated around

oscillation frequency. Even the power supply ripple of the frequency higher than the ADC sampling frequency may fold into the ADC in-band. Hence, it is essential for the LDO to reject a wide range of the power supply ripple, especially at the low-frequency range. In some applications, the LDO should have fast transient response. We noticed that the FMCW frequency hopping approach[12] required an LDO to respond rapidly to the transient load variation. This is because the current consumption of the PLL changes relatively rapidly with the frequency hopping.

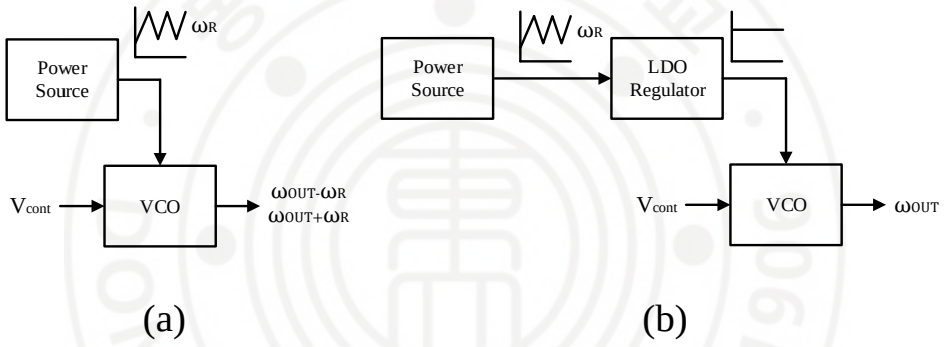


Figure 2.2-1 (a) VCO supplied with power source with ripple and (b) VCO with LDO rejecting power source ripple.

In order to achieve a high PSR across a wide frequency range, various analog circuit techniques have been introduced. A feedforward ripple cancellation achieves a high PSR by combining a feedback and feedforward signal path [13]–[17]. A bandgap reference (BGR) recursive configuration [18] and an output-supplied voltage reference [19] have been proposed to reduce the effect of a non-ideal PSR of the bandgap reference. A multi-loop structure [20]–[24] has been introduced to boost the unity-gain bandwidth and the transient response in various configurations.

2.2.2 LDO for digital systems

Low-power operation of digital processor is critical for all types of applications from mobile SoCs to large-scale datacenter. Dynamic Voltage and Frequency Scaling(DVFS) is widely adopted for optimum power efficiency of digital circuits[25]–[28]. During dynamic voltage scaling, LDO output tracks reference voltage. To minimize idle time during output tracking and optimize performance, LDO output should track reference voltage shift as soon as possible[29]. The DVFS also demands the LDO to scale output voltage down to sub-threshold. During dynamic frequency scaling, current consumption rapidly changes due to sudden change in clock frequency. Memory readout also induce rapid change of current consumption. In these case, the output of LDO should recover quickly after load current step. In both case, DVFS demands LDO to have short transient settling time for both line and load transient. Fully integrated structure with on-chip output capacitor is necessary for monolithic implementation to reduce overall cost. Also, digital processors are fabricated using deeply scaled technologies. Scalable regulation technique is necessary for digital systems. Digital LDO has been suggested as scalable voltage regulator. In [30], digital LDO is synthesized using standard digital library cells and automatic placement-and-routing tools. Event-driven computational digital LDO[31] achieved ultrafast transient response using digital logic gates.

2.2.3 Summary

From different dynamics related to power supply, digital and analog circuit requires designer to set LDO performance priority accordingly. Table 2.2-1 summarizes required performances for analog and digital circuit systems. Each design focus lead to different architecture, device selection/optimization, output capacitance value.

Table 2.2-1 LDO design objective summary.

Analog LDO	Digital LDO
● PSR across wide frequency ● Low output noise voltage ● Good current efficiency	● Low area/power overhead ● Technology scalable ● Fast transient response ● Sub-threshold operation

Chapter 3 Flipped Voltage Follower (FVF) LDO

The flipped voltage follower (FVF) [32] has become one of the most popular analog LDO approaches for the last decade. The FVF LDO has a local feedback loop that reduces output resistance. In addition, an independent control voltage generator can provide an adequate control voltage for the control transistor. However, the transient time of the local feedback loop is relatively slow due to the large pass transistor, and the unity-gain bandwidth of the LDO has been limited. A tri-loop FVF LDO with buffered FVF was proposed to achieve full-spectrum PSR and fast response time in [33]. Although additional loops through a tri-input EA provided more loop gain, the resulting low-frequency PSR was not sufficiently improved. A dual-loop FVF LDO was reported to provide full-spectrum PSR with high low-frequency PSR in [34]. As the control voltage regulating loop was removed, it created another power supply ripple path through the inverting stage, which necessitated an auxiliary LDO.

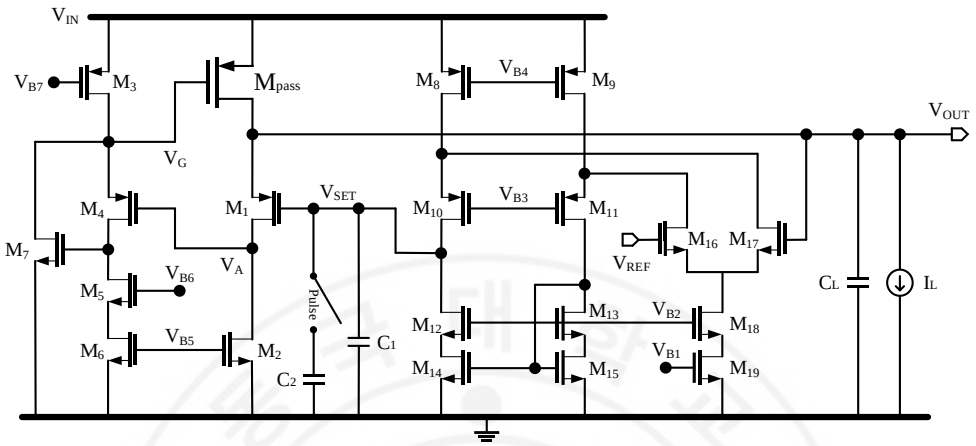
In this thesis, a direct feedback FVF LDO was proposed. By constructing an error amplifier (EA) that directly controls the FVF local loop, the FVF LDO can eliminate the power supply ripple path, resulting in a high PSRR without the need for additional components. A local FVF loop with a super source follower realizes a fast transient response with a unity-gain bandwidth of 469 MHz, and an outer loop incorporating folded cascode EA enhanced a low-frequency PSR to 66 dB. State

matrix decomposition[1] was applied to analyze the stability and parameter sensitivity of a multi-loop FVF LDO.

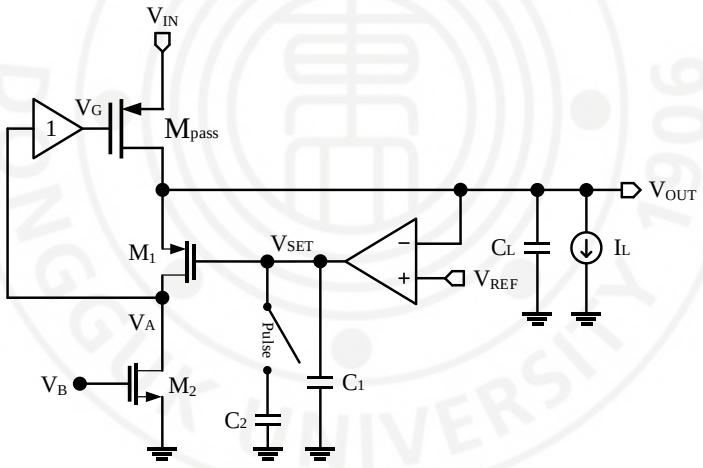
3.1 Direct-Feedback Flipped Voltage Follower LDO

Figure 3.1-1 shows a schematic diagram of the proposed LDO regulator. The LDO consisted of a unity-gain buffer, an error amplifier (EA), an output capacitor, and transistors M_{pass}, M_1, and M_2. M_{pass}, M_1, and M_2 formed a flipped voltage follower. Fast and weak shunt–shunt feedback loop 1 in the flipped voltage follower enables the fast response of the LDO. The output of the error amplifier, V_{SET}, sets the input level of the flipped voltage follower. The input of the EA was connected to the reference input (V_{REF}), and V_{OUT} formed another feedback loop 2. This dramatically enhanced the open loop gain of the overall loop. Since V_{OUT} was directly fed back into EA and the inverting stage was removed, we can eliminate the power supply ripple path without the need for an additional component. To enhance the transient performance, we needed to make the dominant pole of the fast loop 1 located at the output node. The output capacitor, C_L, was connected to the output of the LDO to make the output node of the LDO dominant pole, and the capacitor, C_1, was connected to the output of the error amplifier to stabilize loop 2. An additional compensation capacitor, C_2, was enabled by a start-up pulse generator to guarantee more phase margin during the start-up situation. The unity-gain buffer was to drive the large power transistor, M_{pass}. The size of the transistors, the capacitor values, and

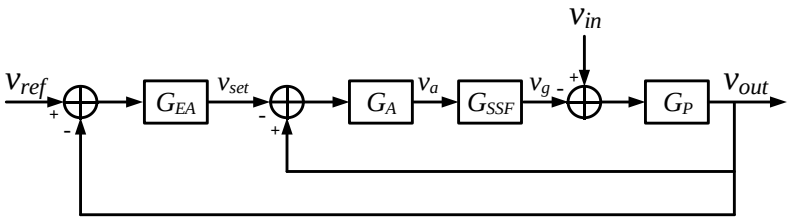
the load current (I_L) values are listed in Table 3.1-1.



(a)



(b)



(c)

Figure 3.1-1 (a) Schematic diagram, (b) simplified schematic diagram, and (c) small-signal block diagram of the proposed FVF LDO.

Table 3.1-1 List of the component values in the proposed FVF LDO.

Component	**Value**	**Component**	**Value**
M_1	8 µm/0.13 µm	M_8, M_9	60 µm/1 µm
M_2	4 µm/0.13 µm	M_{10}, M_{11}	40 µm/1 µm
M_3	14 µm/0.18 µm	M_{12}, M_{13}	12 µm/1 µm
M_4	3 µm/0.06 µm	M_{14}, M_{15}	12 µm/1 µm
M_5, M_6	2 µm/0.18 µm	M_{16}, M_{17}	10 µm/1 µm
M_7	3 µm/0.18 µm	M_{18}, M_{19}	12 µm/1 µm
C_L	350 pF	I_L	1 mA–20 mA

3.1.1 Fast Loop 1 Analysis

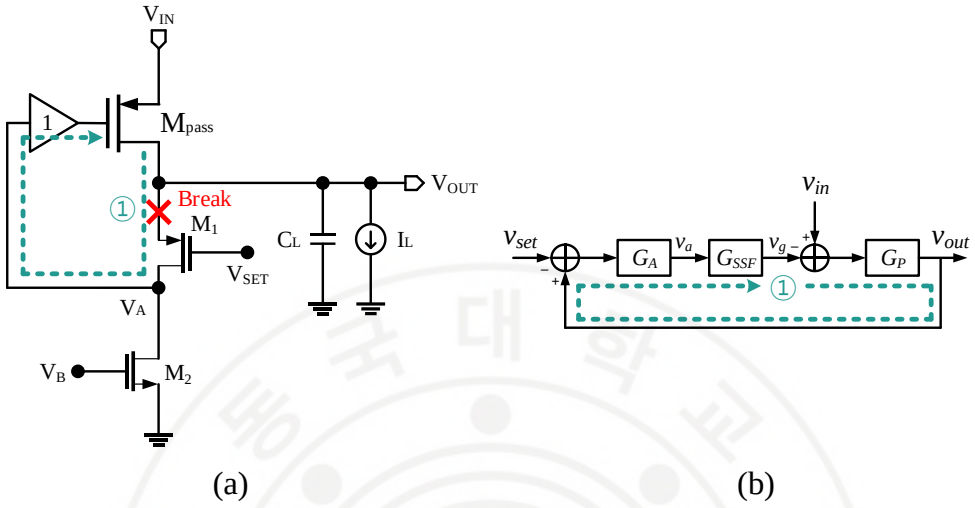


Figure 3.1-2 (a) FVF LDO without loop 2 and (b) its small-signal block diagram.

At higher frequencies where loop 2 did not work, only loop 1 worked. Without loop 2, the LDO simply had the flipped voltage follower (FVF) used as the power stage. The proposed LDO without loop 2 is shown in Figure 3.1-2(a). The input V_{SET} sets the output voltage of the FVF, and any interference or noise in the V_{IN} works as a disturbance for the system. The series-shunt feedback structure reduced the output impedance of the system, enabling a high-frequency operation. The noise or interference from the power source was reduced by the internal feedback loop. To perform the PSRR analysis of the proposed LDO, we established a small-signal block diagram of the LDO. The block diagram is shown in Figure 3.1-2(b). The V_{SET} works as a reference input of the FVF, and any interference or noise in V_{IN} was a

disturbance for the system. The open-loop gain and output of LDO is

$$LG_1 = G_A G_{SSF} G_P \tag{3.1-1}$$

$$v_{out} = \frac{G_A G_{SSF} G_P}{1 + G_A G_{SSF} G_P} v_{set} + \frac{G_P}{1 + G_A G_{SSF} G_P} v_{in} \approx v_{set} + \frac{1}{G_A G_{SSF}} v_{in} \tag{3.1-2}$$

$$G_A = g_{m1}(r_{01} \| r_{02}) \frac{1}{1 + s(r_{o1} \| r_{o2}) C_A} \tag{3.1-3}$$

$$G_{SSF} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.1-4}$$

$$G_P = g_{mP}(R_L \| r_{oP}) \frac{1}{1 + s(R_L \| r_{oP}) C_{OUT}} \tag{3.1-5}$$

where g_{m1} is the transconductance of M_1, r_{o1} and r_{o2} are the output resistance of M_1 and M_2, respectively, C_A is capacitance seen at node A, ω_n is the natural frequency of the super source follower, ζ is the damping factor of the super source follower, g_{mP} is the transconductance of the pass transistor, R_L is the load resistance, r_{oP} is the output resistance of the pass transistor, and C_{OUT} is the capacitance seen at the output node. Supply noise is reduced approximately by G_A at high frequency. The bandwidth of the super source follower was boosted due to the internal feedback structure, and the pole at node A was also at high frequency, as M_1 and M_2 were small. The output capacitor, C_L, was set such that the pass transistor, M_{Pass}, was the slowest working component, and the dominant pole of the controller gain, G_A and G_{SSF}, were placed at a higher frequency. Therefore, loop 1 suppressed the supply noise through a wide frequency range. The supply noise at a higher frequency was

absorbed by the large C_L. The downside of loop 1 was that the open-loop gain was not large. Thus, the resulting PSRR of the LDO may not be sufficient only with loop 1. The error amplifier in loop 2 can improve the PSRR. Phase margin simulation result is shown in Figure 3.1-3. Unity-gain bandwidth of overall loop was 507MHz and phase margin was 37.3˚.

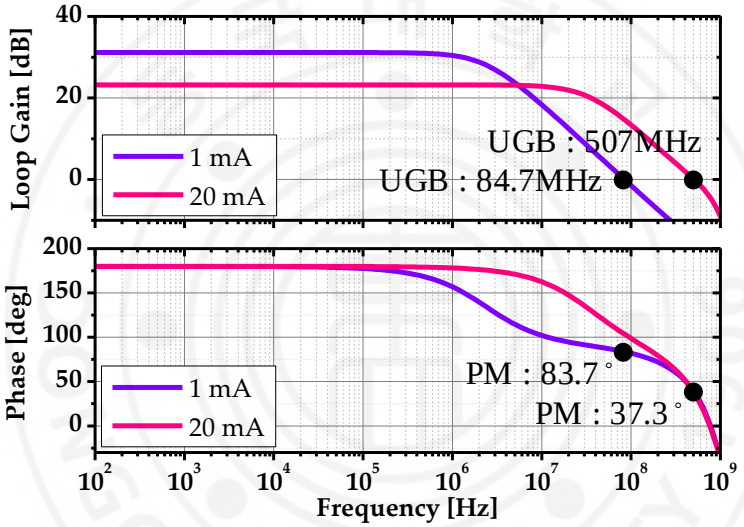


Figure 3.1-3 Open-loop gain simulation result of Loop 1.

3.1.2 Slow Loop 2 Analysis

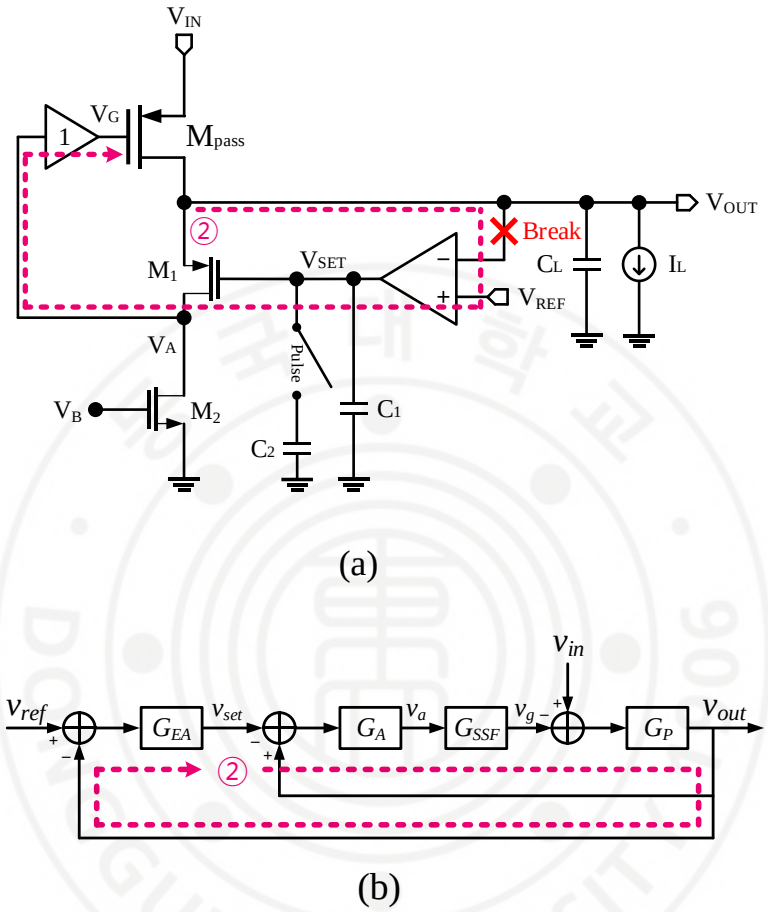


Figure 3.1-4 (a) Slow loop 2 broken at V_{OUT} and (b) Its small-signal block diagram.

The folded cascode amplifier can drastically improve the closed-loop gain. Since V_{OUT} was directly fed back into the EA and the inverting stage was removed, we could eliminate the power supply ripple path without the need for an additional component. Figure 3.1-4 shows the loop 2 feedback path. Breaking the loop at V_{OUT} gives

$$LG_2 = G_{EA}\frac{G_A G_{SSF} G_P}{1 + G_A G_{SSF} G_P} \tag{3.1-6}$$

$$\begin{aligned} v_{out} &= \frac{G_{EA}\frac{G_A G_{SSF} G_P}{1 + G_A G_{SSF} G_P}}{1 + G_{EA}\frac{G_A G_{SSF} G_P}{1 + G_A G_{SSF} G_P}} v_{ref} + \frac{\frac{G_A G_{SSF} G_P}{1 + G_A G_{SSF} G_P}}{1 + G_{EA}\frac{G_A G_{SSF} G_P}{1 + G_A G_{SSF} G_P}} \frac{1}{G_A G_{SSF}} v_{in} \\ &= \frac{G_{EA} G_A G_{SSF} G_P}{1 + (1 + G_{EA}) G_A G_{SSF} G_P} v_{ref} + \frac{G_P}{1 + (1 + G_{EA}) G_A G_{SSF} G_P} v_{in} \\ &\approx v_{ref} + \frac{1}{(1 + G_{EA}) G_A G_{SSF}} v_{in} \end{aligned} \tag{3.1-7}$$

$$G_{EA} = \frac{K_{EA}}{\left(1 + s/\omega_{p1}\right)\left(1 + s/\omega_{p2}\right)} \tag{3.1-8}$$

where G_{EA} is the voltage gain of the folded cascode amplifier. The PSRR is boosted approximately by G_{EA}. Loop 1 is a unity-gain feedback network seen at node V_{SET}, and the unity-gain bandwidth of loop 1 was far beyond that of the EA. Hence, we simply needed to compensate for the folded cascode EA. The folded cascode amplifier can be stabilized simply by adding the compensation capacitor, C_1, to the output of the amplifier. Phase margin simulation result is shown in Figure 3.1-5. Bandwidth of overall loop was 31.2MHz and phase margin was 63.6˚.

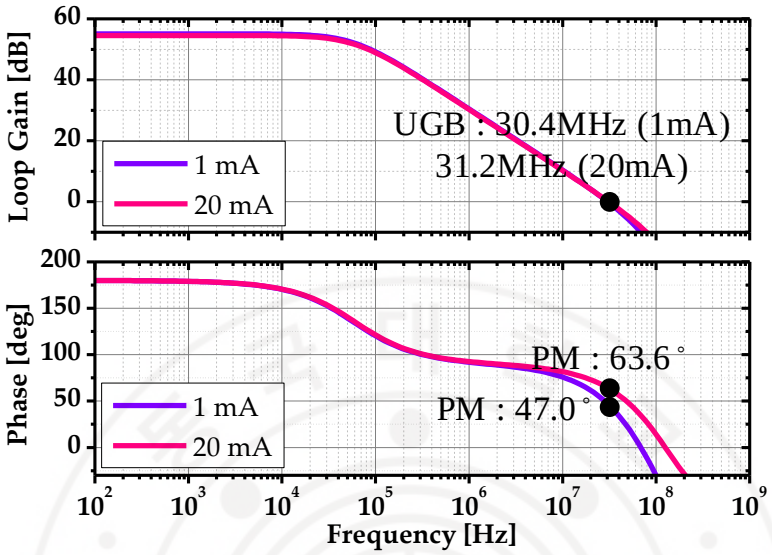
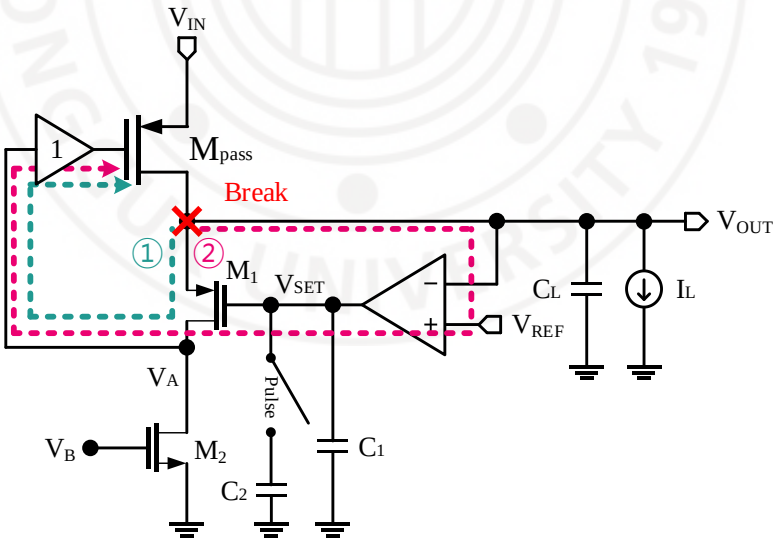
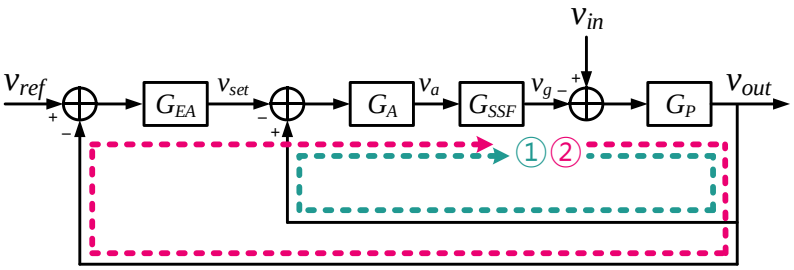


Figure 3.1-5 Open-loop gain simulation result of slow loop 2.

3.1.3 Overall loop analysis



(a)



(b)

Figure 3.1-6 (a)FVF LDO overall loop (b) its simplified block diagram.

Loop 1 and Loop 2 formed a combined global loop. The global loop had the largest closed-loop gain, making it critical for the phase margin design. Figure 3.1-6 shows the combined diagram of loop 1 and loop 2. By breaking the loop at the node V_{OUT}, the output voltage is expressed as

$$LG = (1 + G_{EA})G_A G_{SSF} G_P \tag{3.1-9}$$

$$v_{out} = \frac{(1 + G_{EA})G_A G_{SSF} G_P}{1 + (1 + G_{EA})G_A G_{SSF} G_P} v_{ref} + \frac{G_P}{1 + (1 + G_{EA})G_A G_{SSF} G_P} v_{in} \approx v_{ref} + \frac{1}{(1 + G_{EA})G_A G_{SSF}} v_{in} \tag{3.1-10}.$$

Here, the open-loop gain had a dominant pole at the output of the EA, and the second pole was at the output of the LDO. The $(1 + G_{EA})$ term in (11) made a quadratic zero near the unity-gain bandwidth of the EA. This zero was set to cancel out the second pole, which was below the unity-gain bandwidth of the LDO. It was noted that the LDO would be unstable without this zero. As a result, the $(1 + G_{EA})$ term boosted the unity-gain bandwidth of the LDO. Figure 3.1-7 shows the phase

margin simulation result. The unity-gain bandwidth of the overall loop was 469 MHz, and the phase margin was 44.1°.

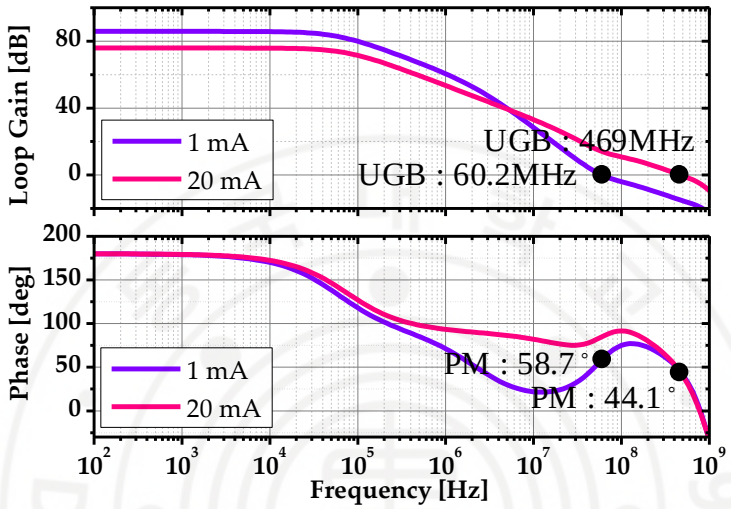


Figure 3.1-7 Open-loop gain simulation result of overall loop.

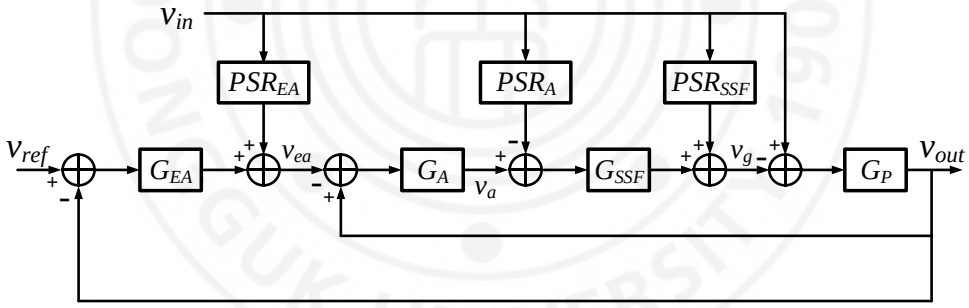
3.1.4 Effect of non-ideal PSRR of each components

There was more than one power supply ripple path in the FVF LDO. Circuit blocks with a non-ideal PSRR can provide an additional path for the power supply ripple. shows the effect of non-ideal components on PSRR. With the simplified model, the output of the LDO is given as

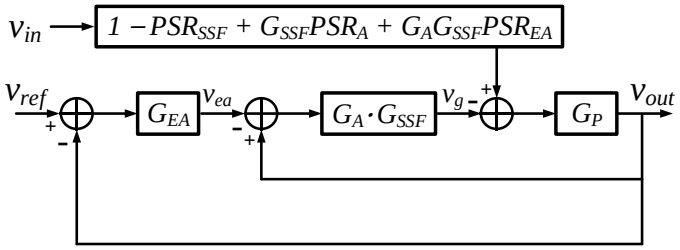
$$v_{out} = \frac{(1+G_{EA})G_A G_{SSF} G_P}{1+(1+G_{EA})G_A G_{SSF} G_P} v_{ref} + \frac{G_P}{1+(1+G_{EA})G_A G_{SSF} G_P} \begin{pmatrix} 1 - PSRR_{SSF} + G_{SSF} PSRR_A \\ + G_A G_{SSF} PSRR_{EA} \end{pmatrix} v_{in} \quad (3.1\text{-}11)$$

$$\approx v_{ref} + \frac{\alpha}{(1+G_{EA})G_A G_{SSF}} v_{in}$$

where PSR_{SSF} is the power supply rejection of the super source follower, PSR_A is the power supply rejection of the FVF stage, and PSR_{EA} is the power supply rejection of the folded cascode amplifier. The PSRR of the FVF stage and EA should be as low as possible. On the other hand, the super source follower with a poor PSRR helps the LDO reject the power supply ripple by working as a feedforward path



(a)



(b)

Figure 3.1-8 (a)Small-signal block diagram of FVF LDO including the effect of nonideal PSR and (b)its simplified model.

3.2 Stability analysis of FVF LDO

Since the proposed LDO has two feedback loops, state matrix decomposition[1] must be more suitable for analyzing the stability than a classical open-loop ac analysis. Without looking at each loop separately, the closed-loop analysis is given below.

Let $X_1 = v_{set}/K_{EA}$ be a state variable, and the gain of the error amplifier is

$$G_{EA} = \frac{v_{set}}{v_{ref} - v_{out}} = \frac{K_{EA}}{\left(1+s/\omega_{p1}\right)\left(1+s/\omega_{p2}\right)}. \qquad (3.2\text{-}1)$$

Substituting $v_{set} = K_{EA}X_1$ into (3.2-1) and identifying the numerator and the denominator,

$$v_{ref} - v_{out} = X_1 + \left(1/\omega_{p1} + 1/\omega_{p2}\right)\dot{X}_1 + 1/\omega_{p1}\omega_{p2}\ddot{X}_1. \qquad (3.2\text{-}2)$$

Let a state variable $X_2 = \dot{X}_1$, and when substituting it into (3.2-2),

$$\dot{X}_2 = -\omega_{p1}\omega_{p2}X_1 - \left(\omega_{p1}+\omega_{p2}\right)X_2 - \omega_{p1}\omega_{p2}v_{out} + \omega_{p1}\omega_{p2}v_{ref}. \qquad (3.2\text{-}3)$$

Let $X_3 = v_a/K_A$ be a state variable, and the gain of the error amplifier is

$$G_A = \frac{v_a}{v_{ref} - v_{set}} = \frac{K_A}{1 + s/\omega_A}. \quad (3.2\text{-}4)$$

Substituting $v_a = K_A X_3$ into (3.2-4) and identifying the numerator and the denominator,

$$\dot{X_3} = -K_{EA}\omega_A X_1 - \omega_A X_3 + \omega_A v_{out}. \quad (3.2\text{-}5)$$

Let $X_4 = v_g/K_{SSF}$ be a state variable, and the gain of the super source follower is

$$G_{SSF} = \frac{v_g}{v_a} = \frac{K_{SSF}}{1 + 2\zeta/\omega_n s + 1/\omega_n^2 s^2}. \quad (3.2\text{-}6)$$

Substituting $v_g = K_{SSF} X_4$ into (3.2-6) and identifying the numerator and the denominator,

$$v_a = K_A X_3 = X_4 + 2\zeta/\omega_n \dot{X}_4 + 1/\omega_n^2 \ddot{X}_4. \quad (3.2\text{-}7)$$

Let a state variable $X_5 = \dot{X}_4$, and when substituting it into (3.2-7),

$$\dot{X}_5 = \omega_n^2 K_A X_3 - \omega_n^2 X_4 - 2\zeta\omega_n X_5. \quad (3.2\text{-}8)$$

Let $X_6 = v_{out}/K_P$ be a state variable, and the gain of the pass transistor is

$$G_P = \frac{v_{out}}{v_{sgP}} = \frac{K_P}{1 + s/\omega_P}. \quad (3.2\text{-}9)$$

Assuming the PSR of each component is constant, the effective source-gate voltage v_{sgP} is

$$v_{sgP} = (1 - PSR_{SSF} + K_{SSF} PSR_A + K_A K_{SSF} PSR_{EA}) v_{in} - v_g. \quad (3.2\text{-}10)$$

Substituting (3.2-10), $v_{out} = K_P X_6$ and $v_g = K_{SSF} X_4$ into (3.2-9), and identifying

the numerator and the denominator,

$$\begin{aligned}\dot{X}_6 &= -K_{SSF}\omega_P X_4 - \omega_P X_6 \\ &\quad + \omega_P(1 - PSR_{SSF} + K_{SSF}PSR_A + K_A K_{SSF}PSR_{EA})v_{in}.\end{aligned} \tag{3.2-11}$$

Substituting $v_{out} = K_P X_6$ into (3.2-3) and (3.2-5), we finally obtain

$$\begin{cases}\dot{X}_1 = X_2 \\ \dot{X}_2 = -\omega_{p1}\omega_{p2}X_1 - (\omega_{p1} + \omega_{p2})X_2 - \omega_{p1}\omega_{p2}K_P X_6 + \omega_{p1}\omega_{p2}v_{ref} \\ \dot{X}_3 = -K_{EA}\omega_A X_1 - \omega_A X_3 + \omega_A K_P X_6 \\ \dot{X}_4 = X_5 \\ \dot{X}_5 = \omega_n^2 K_A X_3 - \omega_n^2 X_4 - 2\zeta\omega_n X_5 \\ \dot{X}_6 = -K_{SSF}\omega_P X_4 - \omega_P X_6 + \omega_P(1 - PSR_{SSF} + K_{SSF}PSR_A + K_A K_{SSF}PSR_{EA})v_{in}\end{cases} \tag{3.2-12}$$

$$\begin{cases}X_1 = v_{set}/K_{EA} \\ X_2 = \dot{X}_1 \\ X_3 = v_a/K_A \\ X_4 = v_g/K_{SSF} \\ X_5 = \dot{X}_4 \\ X_6 = v_{out}/K_P\end{cases} \tag{3.2-13}$$

$$\begin{cases}v_{set} = K_{EA}X_1 \\ v_a = K_A X_3 \\ v_g = K_{SSF}X_4 \\ v_{out} = K_P X_6\end{cases} \tag{3.2-14}$$

We have two inputs v_{in}, v_{ref} and four outputs v_{set}, v_a, v_g, and v_{out}. The state space model of LDO with six state variables is

$$\begin{bmatrix}\dot{X}_1\\ \dot{X}_2\\ \dot{X}_3\\ \dot{X}_4\\ \dot{X}_5\\ \dot{X}_6\end{bmatrix}$$

$$= \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 \\ -\omega_{p1}\omega_{p2} & -\omega_{p1}-\omega_{p2} & 0 & 0 & 0 & -\omega_{p1}\omega_{p2}K_p \\ -K_{EA}\omega_A & 0 & -\omega_A & 0 & 0 & \omega_A K_p \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & \omega_n^2 K_A & -\omega_n^2 & -2\zeta\omega_n & 0 \\ 0 & 0 & 0 & -K_{SSF}\omega_p & 0 & -\omega_p \end{bmatrix} \begin{bmatrix} X_1\\ X_2\\ X_3\\ X_4\\ X_5\\ X_6 \end{bmatrix} \quad (3.2\text{-}15)$$

$$+ \begin{bmatrix} 0 & 0 \\ 0 & \omega_{p1}\omega_{p2} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ \omega_p(1-PSR_{SSF} + K_{SSF}PSR_A + K_A K_{SSF} PSR_{EA}) & 0 \end{bmatrix} \begin{bmatrix} v_{in} \\ v_{ref} \end{bmatrix}$$

$$\begin{bmatrix} v_{set} \\ v_a \\ v_g \\ v_{out} \end{bmatrix} = \begin{bmatrix} K_{\mathrm{EA}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & K_{\mathrm{A}} & 0 & 0 & 0 \\ 0 & 0 & 0 & K_{SSF} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & K_{\mathrm{p}} \end{bmatrix} \begin{bmatrix} X_1\\ X_2\\ X_3\\ X_4\\ X_5\\ X_6 \end{bmatrix}. \quad (3.2\text{-}16)$$

The LDO is asymptotically stable when all the real parts of the eigenvalues of matrix A are negative. The eigenvalues are given as

$$\begin{aligned} \lambda_1 &= -5.543 \cdot 10^9 + j4.612 \cdot 10^9 \\ \lambda_2 &= -5.543 \cdot 10^9 - j4.612 \cdot 10^9 \\ \lambda_3 &= -1.414 \cdot 10^9 + j4.342 \cdot 10^9 \\ \lambda_4 &= -1.414 \cdot 10^9 - j4.342 \cdot 10^9 \\ \lambda_5 &= -3.444 \cdot 10^8 + j2.297 \cdot 10^8 \\ \lambda_6 &= -3.444 \cdot 10^8 - j2.297 \cdot 10^8 \end{aligned} \quad (3.2\text{-}17)$$

Since all the eigenvalues have negative real parts, the LDO was asymptotically stable. The parameters used in the analysis are given in Table 3.2-1. The parameters were extracted from the circuit simulation results, including parasitics. Figure 3.2-1 compares the PSRR simulation results from the circuit simulator and state space model. The state space model fits the circuit simulation result and can predict the pole/zero location of the transfer function.

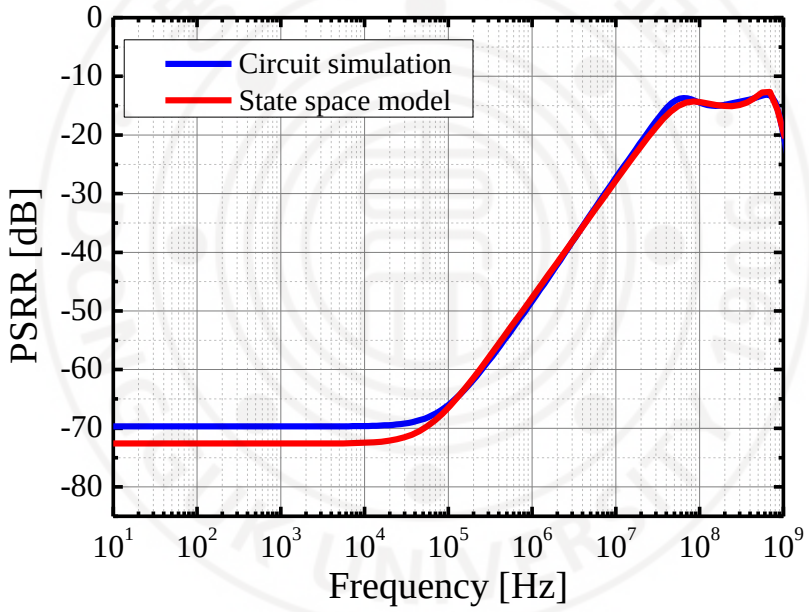


Figure 3.2-1 PSRR simulation of the proposed LDO.

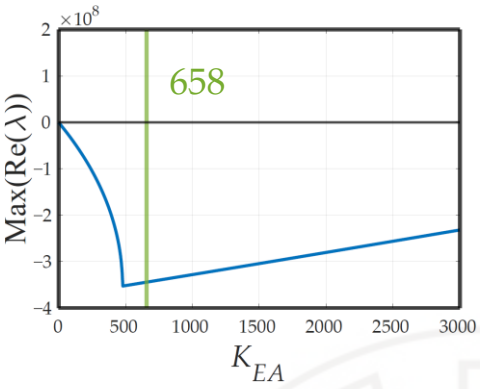
Table 3.2-1 Parameters used in the state space model

Parameter	Value	Parameter	Value
K_{EA}	657.9	K_A	12.576
ω_{p1}	$2\pi \cdot 5.698 \cdot 10^4$	ω_A	$2\pi \cdot 1.058 \cdot 10^9$
ω_{p2}	$2\pi \cdot 1.194 \cdot 10^8$	PSR_A	0.02778
PSR_{EA}	0.05833	K_{sf}	0.8386
K_p	3.178	ω_n	$2\pi \cdot 1.181 \cdot 10^9$
ω_p	$2\pi \cdot 1.363 \cdot 10^7$	ζ	0.4799
		PSR_{sf}	0.0104

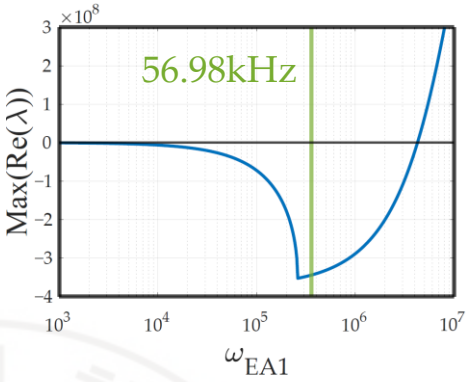
The red line represents the simulation result with the state space model, and the blue line represents the simulation result with Cadence Spectre. We also identified the parameter variation sensitivity by computing the real part of the critical eigenvalue with variation in each parameter. Plotting the highest real part of the eigenvalues, the circuit should follow the conditions:

$$\forall \lambda_i, \mathrm{Re}(\lambda_i) < 0 \qquad (3.2\text{-}18)$$

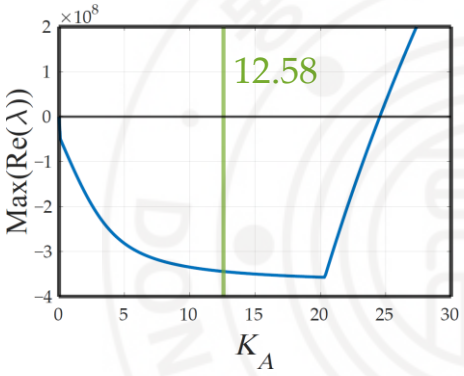
Figure 3.2-2 shows parameter variation sensitivity simulation results with various circuit parameters. Nominal design values are marked as the green line.


658
Max(Re(λ))
K_{EA}

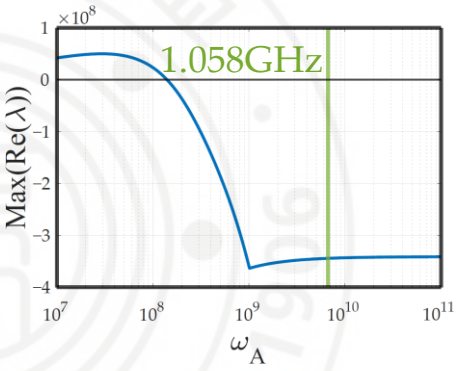
(a)


56.98kHz
Max(Re(λ))
ω_{EA1}

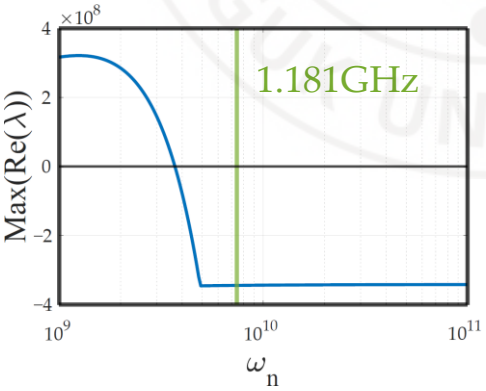
(b)


12.58
Max(Re(λ))
K_A

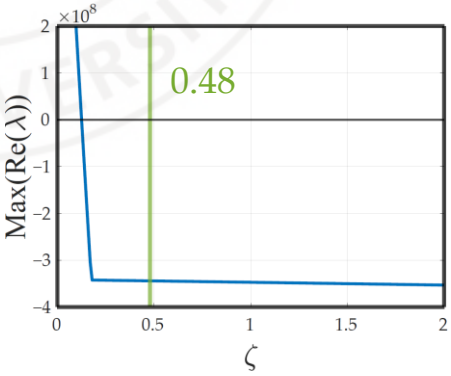
(c)


1.058GHz
Max(Re(λ))
ω_A

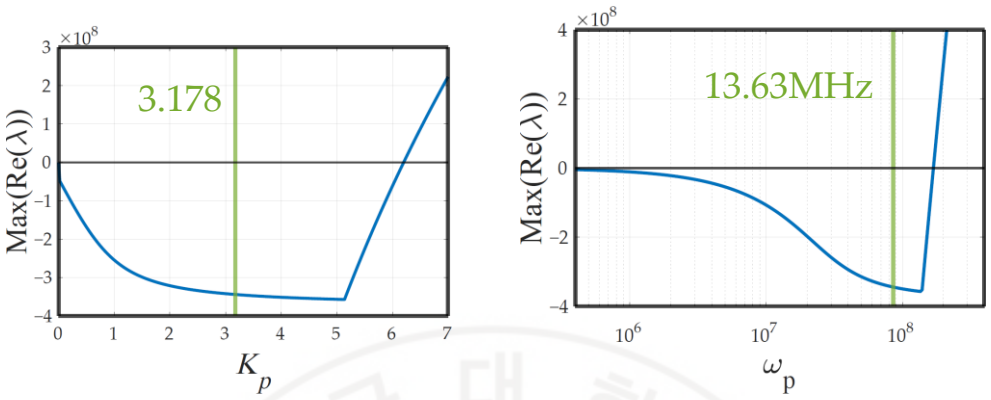
(d)


1.181GHz
Max(Re(λ))
ω_n

(e)


0.48
Max(Re(λ))
ζ

(f)



(g) (h)

Figure 3.2-2 Parameter sensitivity simulation result for (a)voltage gain of folded cascode EA, (b)dominant pole at folded cascode EA, (c)voltage gain of FVF stage, (d)pole at FVF stage, (e)natural frequency of SSF, (f)damping factor of SSF, (g)voltage gain of pass transistor, (h)pole at output.

3.3 Measurement result

We implemented the LDO in TSMC 65 nm CMOS technology with an active area of 0.037 mm^2, including a 350 pF on-chip output capacitor. Figure 3.3-1 shows a chip photograph of a fabricated FVF LDO. A 350 pF output capacitor was implemented on-chip using a MOM capacitor. We performed the on-chip probe measurements and the chip-on-board measurements.

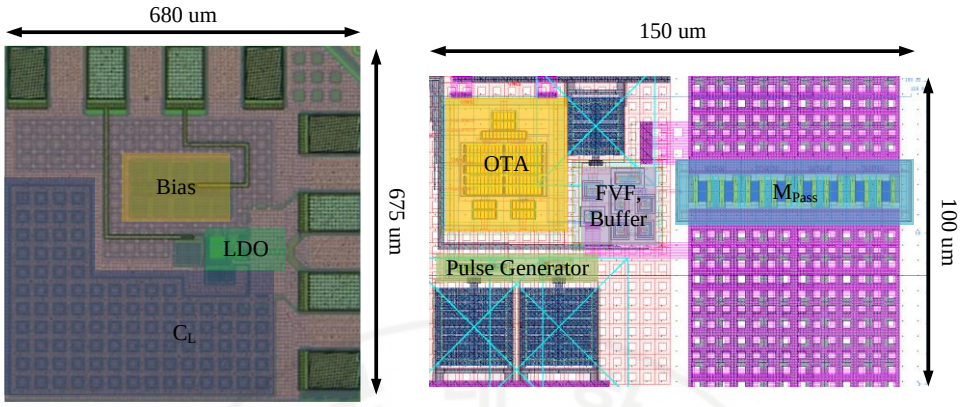
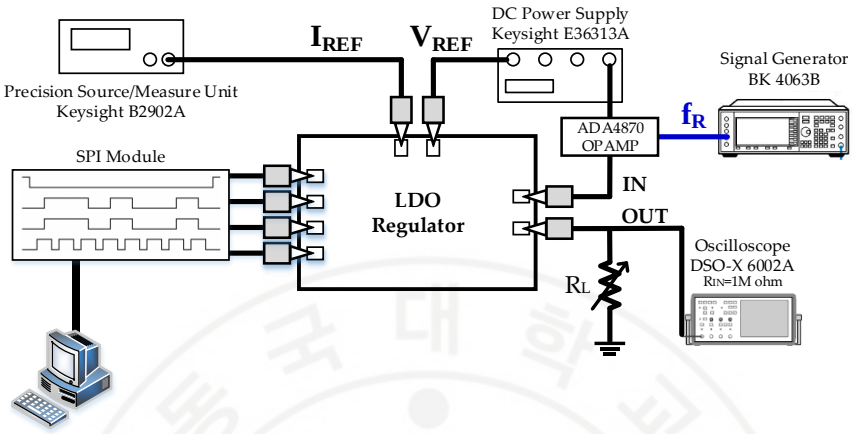


Figure 3.3-1 (a) Chip photograph of the fabricated FVF LDO and (b) layout of the FVF LDO.

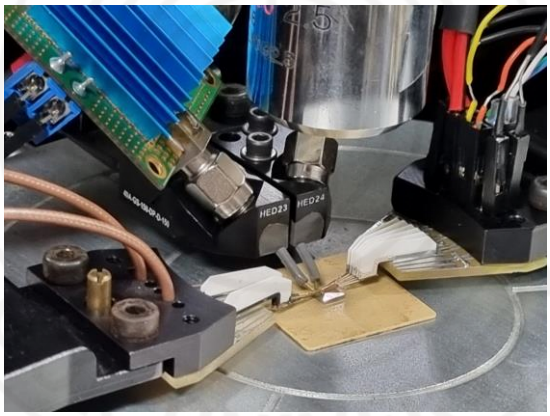
3.3.1 Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio measurement setting is shown in Figure 10. The Analog Device ADA4870 OPAMP supplied the DC power and ac ripple at the frequency of f_R to the LDO. The OPAMP was used to reduce the output impedance and combine the DC voltage with the ac ripple. A Keysight E36313A DC power supply sets the reference voltage and voltage bias for the OPAMP. A BK Precision BK4063B arbitrary signal generator provided the input ripple signal to the OPAMP. A Keysight B2902A SMU supplied I_{ref} to bias the internal amplifiers and buffer. The biasing point was controlled by the SPI Module. A Keysight DSO-X oscilloscope was used to measure the input and output ripple. The PSRR was calculated using measured input and output. Figure 11 shows the PSRR measurement result. The fabricated FVF LDO achieved a full-spectrum PSR of 64.6 dB at 100 kHz and the

worst measured PSRR of 10 dB at 200 MHz.



(a)



(b)

Figure 3.3-2 (a) Schematic diagram of the PSRR measurement setting and (b) a photograph of the measurement setting.

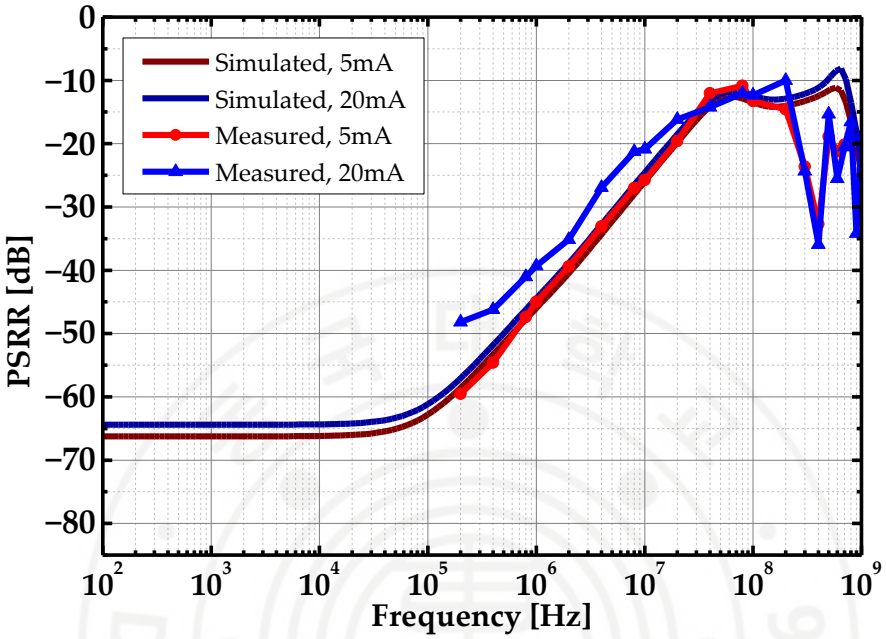
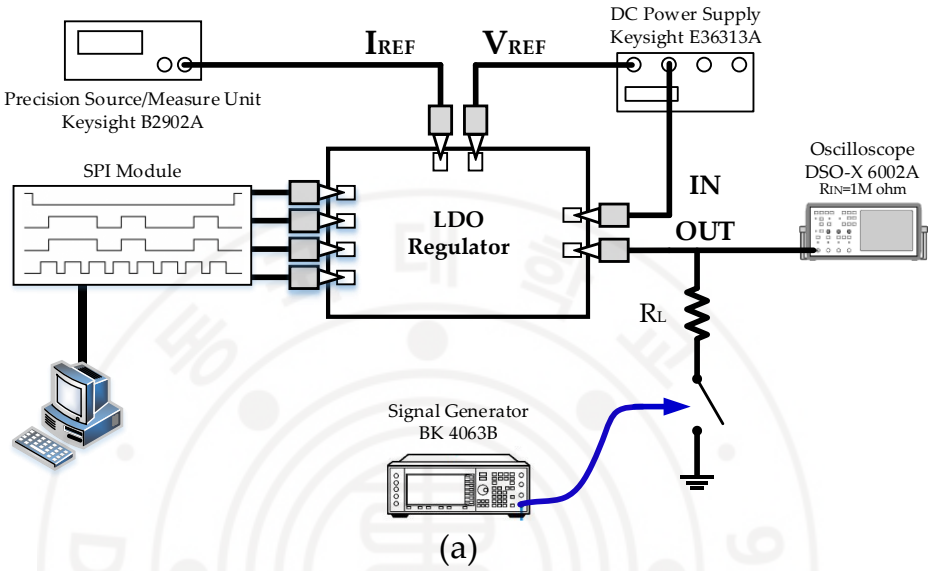


Figure 3.3-3 Simulated and measured PSRR of the FVF LDO.

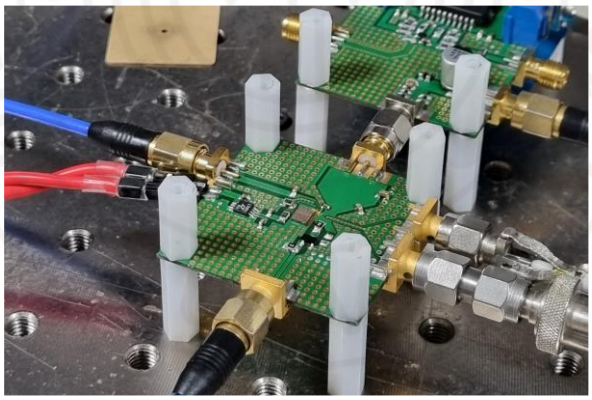
3.3.2 Transient Response

The load transient measurement setting is shown in Figure 3.3-4. A Keysight E36313A was used to supply V_{IN} and V_{REF} to the LDO, and a Keysight B2902A was used to input I_{REF} to bias the internal amplifiers and buffer. The load control signal was given from the BK precision BK4064B arbitrary signal generator. The load current was stepped from minimum to maximum, with an edge time of 8 ns. The load transient measurement result is given in Figure 3.3-5. The maximum voltage droop was 30.3 mV, and the settling time was about 16 ns. Transient load regulation

was 141 μV/mA.



(a)



(b)

Figure 3.3-4 (a) Schematic diagram of the load transient measurement setting and (b) a photograph of the measurement setting.

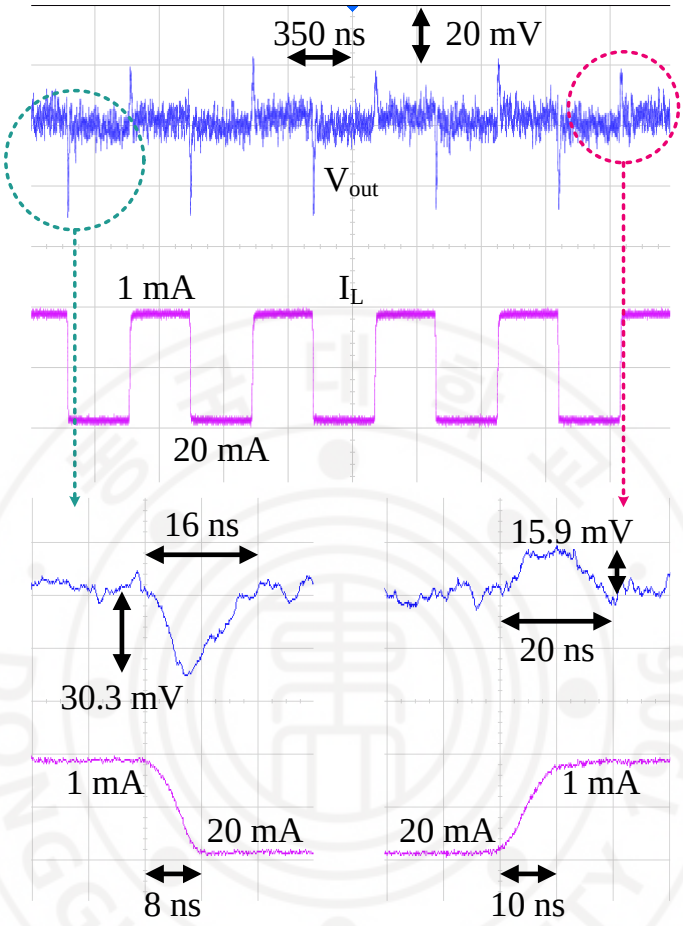


Figure 3.3-5 Load transient measurement result.

The line transient measurement setting was the same as the PSRR measurement setting, and the only difference was that the ripple signal, f_R, was replaced with a square wave. The line transient measurement result is given in Figure 3.3-6. With the power supply voltage changing from 1.2 V to 1.4 V within 20 ns, the output voltage changed by about 25.7 mV. The settling time to the final value was about 40 ns.

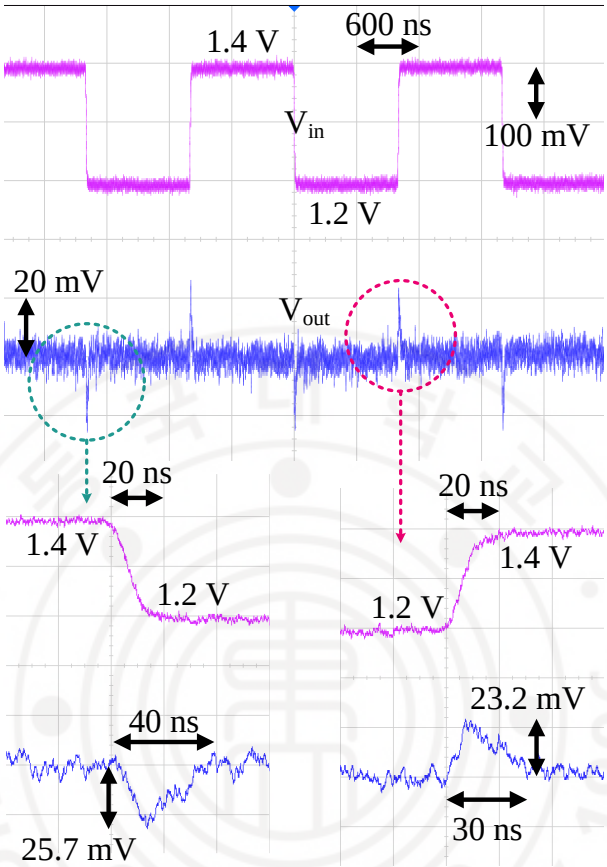


Figure 3.3-6 Line transient measurement result.

3.3.3 Discussion

Table 3.3-1 summarizes the performance of the proposed FVF LDO with other state-of-the-art LDOs. The proposed FVF LDO occupied a 0.037 mm^2 active area. The LDO output was 1 VDC with a supply voltage of 1.2 VDC. The maximum output current was 20 mA, and the quiescent current was 290 µA. An output capacitor of 350 pF was used. The worst-case load transient overshoot was 30.3 mV

with a load current step of 8 ns edge time, and the output was settled within 16 ns. When the response time of the LDO is comparable to the edge time, the assumption in the simple response time equation [35] is no longer valid. Assuming that the load current varies at a constant rate[36], the response time is given as

$$T_R = \sqrt{\frac{2C_L \Delta V_o T_{edge}}{\Delta I_L}} \tag{3.3-1}$$

The shorter the response time, the better the performance is. The response time, calculated according to (3.3-1), is shown in Table 3.3-1. The response time of the LDO was 2.99 ns. Transient FoM [35] is given by

$$\text{FoM} = T_R \frac{I_Q}{I_{L(max)}} \tag{3.3-2}$$

where the smaller FoM represents better performance. The proposed FVF LDO achieved an FoM of 43.4 ps. The low-frequency PSRR of the FVF LDO was 66 dB, and the worst-measured PSRR of the LDO was 10 dB at 200 MHz.

Table 3.3-1 Performance comparison with state-of-the-art LDOs.

LDO	This Work	[34]	[13]	[36]
Type	Analog	Analog (FVF)	Analog (FFRC)	Analog (OCL)
Process [nm]	65	65	130	130
Area [mm^2]	0.037	0.053	0.049	0.008
V_{in} [V]	1.2	1.2	1.15	1-1.4
V_{out} [V]	1	1	1	0.8
I_Q [uA]	290	27-82	50	112
Max. I_{load} [mA]	20	20	25	25
Load capacitor [nF]	0.35	0.3	4000	0.025
Load transient Overshoot [mV]	30.3 @8ns step	71 @0.8ns step	15 @10ns step	48 @3ns step
Settling Time @Max. current step [ns]	16	200	500	80
T_R [ns]	2.99	1.31	219	0.197
Transient FoM [ps]	43.4	1.45	438	0.9
Settling Time	16	200	500*	80
PSRR [dB]	66.2 @1kHz† 43.5 @1MHz 23.5 @10MHz	60 @1kHz 42 @1MHz 10 @100MHz	60 @1kHz 67 @1MHz	63 @1kHz 57 @1MHz 22 @10MHz
Load regulation [uV/mA]	141	15	48	173
Line Regulation [mV/V]	1.04	1	26	2.25

* Estimated from figure. † Simulated.

The proposed FVF LDO was successfully implemented in 65 nm CMOS technology. The PSRR measurement results confirmed that the analytic model and simulation results corresponded quite well with the measured PSRR. Our work has demonstrated that a simple direct feedback structure could improve low-frequency PSRR without additional components. The proposed LDO operated stably with various line/load transient situations, and the output settled rapidly to the final value. For future research, current efficiency can be improved by using an efficient buffer structure or an adaptive bias scheme.

Chapter 4 Ring LDO

Digital LDOs were considered to be a scalable regulation solution for digital systems, due to its ability to regulate with wide range of input/output voltage, being able to adapt well into deeply scaled technologies. Despite active researches, digital LDO has not been able to achieve regulation performance that was considered average for analog LDOs. Event-driven PI control[37], [38] achieved good current efficiency, but the output capacitor value (0.4nF, 0.1nF) was too large considering maximum load current(3.5mA, 2.8mA). Unary pass transistor array with linear controller and residue-tracking loop[39] enabled accurate line/load regulation without large output capacitor, but linear controller was still not able to respond rapidly to load current variation. Computational LDO[31], [40] achieves fast transient settling time at the cost of consuming large quiescent current up to staggering 2.4mA, which does not change appreciably with load current.

Though digital processors are more robust to power source ripple than analog systems, a variation in supply voltage can induce timing mismatch, which can reduce frequency margin for high-performance processor. Moreover, in subthreshold operation, time delay and maximum operating frequency varies significantly with supply voltage[41], [42]. LDO should also provide accurate supply voltage and reject power supply ripple. Power source rejection of digital LDO highly depends on ADC sampling rate or control mechanism, and output accuracy is limited by ADC

resolution. Many digital regulation techniques cannot reject the power source ripple if the magnitude of the ripple is below certain threshold.

These tragedies are mainly from absence of analog amplification techniques. The Basic analog amplifiers and operation transconductance amplifier (OTA) are not suitable for deeply scaled technology. Ring amplifier is considered to be a next-generation analog amplifier[43]. Intrinsically unstable ring oscillator is stabilized by dead zone biasing. Recent researches demonstrated high-accuracy, fast slewing, compact and scalable characteristics of ring amplifiers with pipelined ADCs[44]-[48], ringamp-based LDOs[49], [50].

4.1 Ring Amplifier

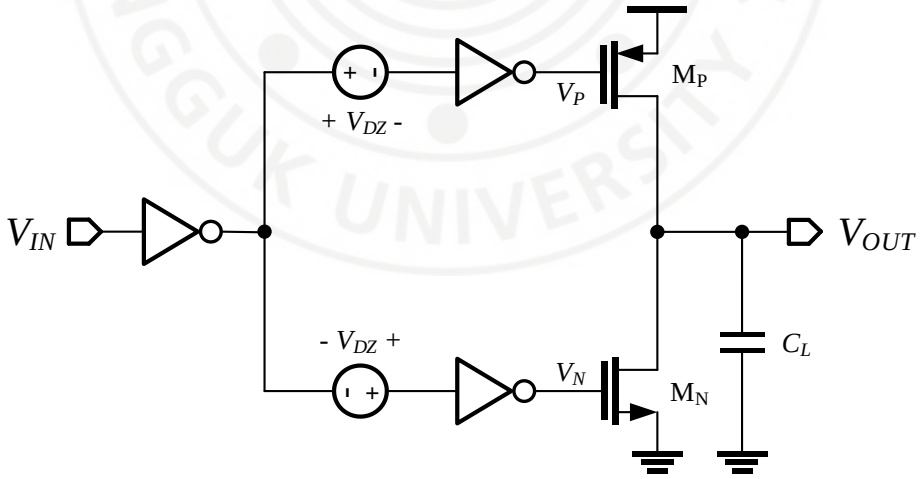


Figure 4.1-1 Schematic Diagram of Basic Ring amplifier.

Basic three-stage ring amplifier is shown on Figure 4.1-1. The ring amplifier consists of three cascaded CMOS inverter with second stage split into two signal paths. Dead zone bias voltage V_{DZ} is applied before second stage. The typical short-circuit output current of ring amplifier is described on Figure 4.1-2. With sufficient dead-zone biasing, the last stage of amplifier is shut down. This ringamp configuration is often called class-B ring amplifier. The input voltage range at which the amplifier is shut down is dead-zone. Weak-zone follows dead-zone, where the last stage is in weak inversion. The input-referred dead-zone V_{DZi} is

$$V_{in}^{'} = V_{in} - V_M \tag{4.1-1}$$

$$V_{DZi} = \frac{V_{DZ}}{A_1} \tag{4.1-2}$$

where V_M is inverter threshold and A_2 is the voltage gain of first stage. Generally the amplifier has high voltage gain and slew rate, as it uses most of the advantage of scaled CMOS technology, but the ring amplifier is very nonlinear and operating speed heavily depends on input signal.

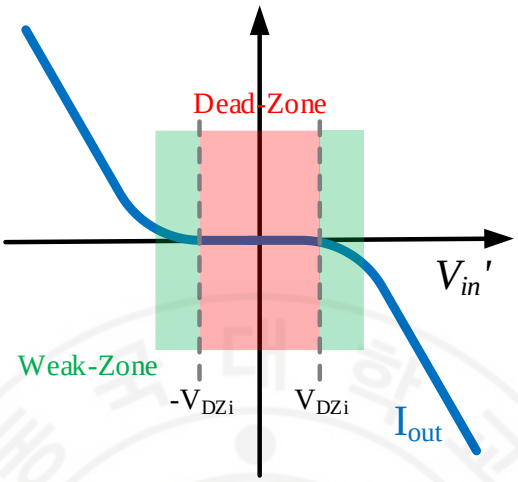


Figure 4.1-2 Typical short-circuit output current of ring amplifier.

Ring amplifier exhibits very special characteristics when it is put in feedback configuration. Ring amplifier inside a switched-capacitor feedback structure is shown in Figure 4.1-3. Without dead-zone biasing, the circuit is simply a ring oscillator. It achieves excellent open-loop gain, unity-gain bandwidth, and slew rate, except it is unstable. The circuit is stabilized through moving the pole at output to lower frequency with sufficient dead-zone biasing using capacitors. The last stage is totally slowed down because the transistors M_P and M_N is shut down. During transient situation, the transistors are turned on again and slewing efficiency is restored. Typical transient response of switched-capacitor ring amplifier is shown on Figure 4.1-4. Initially, the amplifier fully turn on/off the M_P and M_N, which leads to efficient and rapid slewing with slew current I_{RAMP}. The output ramps into desired value. Once the fed back signal V_A reaches lower boundary of input-referred dead-

zone, the amplifier should stop slewing. But the slewing continues because of nonzero delay τ_d. The overshoot voltage is expressed as

$$V_{ovs} = \frac{I_{RAMP}\tau_d}{C_L}$$
$$V_A = V_M - V_{DZi} + \frac{C_2}{C_1+C_2}\frac{I_{RAMP}\tau_d}{C_L}. \quad (4.1\text{-}2)$$

The output voltage does not change until discharging starts. Discharging starts τ_d after V_A reaches upper boundary of input-referred dead-zone. The effective output error is decreased by V_{DZi}. As shown in Figure 4.1-2, the ramp current depends on the difference of V_A and input-referred dead-zone. Therefore, the discharge current during discharge is smaller than initial ramping current and overshoot voltage is progressively decreased. This process repeats until overshoot voltage arrive at input-referred dead-zone. Then, the output reaches steady-state and follows small-signal stability. For the output to reach steady-state,

$$-V_{DZi} \le \frac{C_2}{C_1+C_2}\frac{I_{RAMP}\tau_d}{C_L} - V_{DZi} \le V_{DZi}$$
$$\frac{C_2}{C_1+C_2}\frac{I_{RAMP}\tau_d}{C_L} \le 2V_{DZi}. \quad (4.1\text{-}3)$$

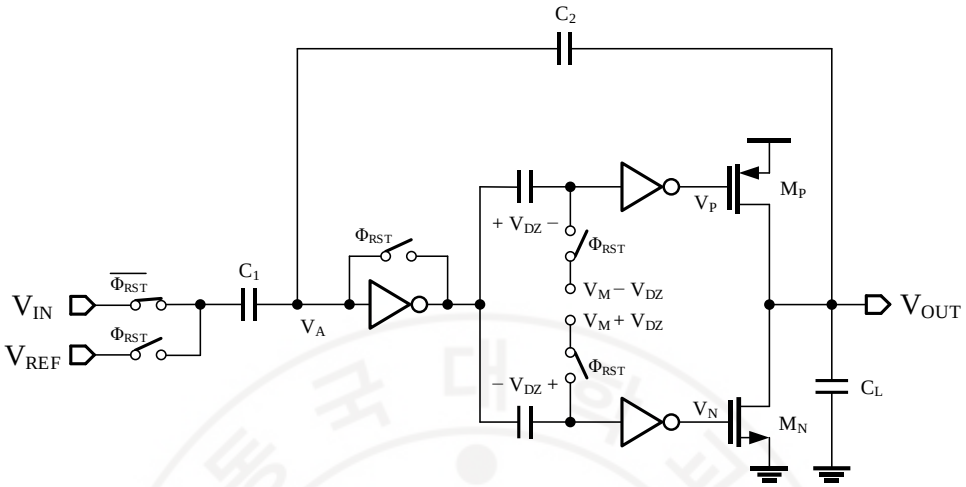


Figure 4.1-3 Ring amplifier in a switched-capacitor feedback configuration.

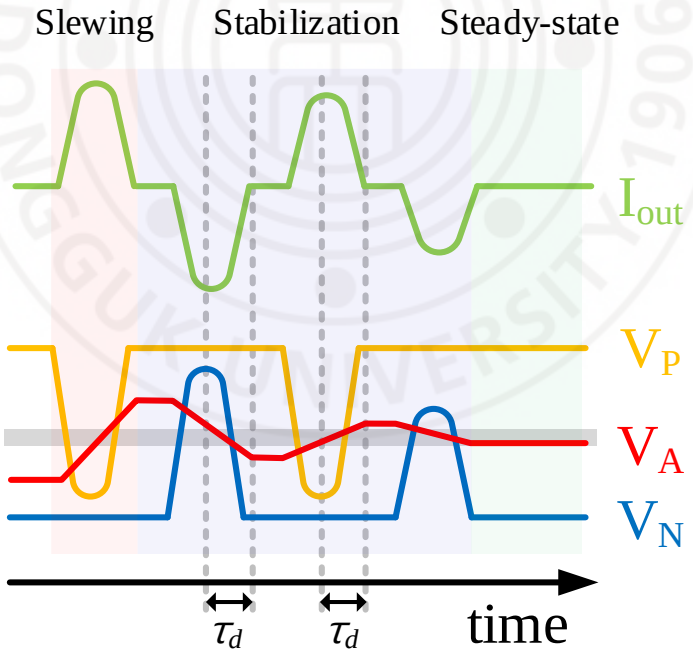


Figure 4.1-4 Typical transient waveform of switched-capacitor ring amplifier.

We can take advantage of fast transient response of ring amplifier when ring amplifier is an error amplifier of LDO. A low-dropout regulator incorporating a ring amplifier as an error amplifier is exemplified in Figure 4.1-5. With sufficient dead-zone biasing, the amplifier is shut down when it is in steady-state. With V_G being slowest operating node, the regulator is stabilized around dead-zone. The steady-state error of LDO is

$$V_{DZi} = \frac{V_{DZ}}{A_1} \tag{4.1-4}$$

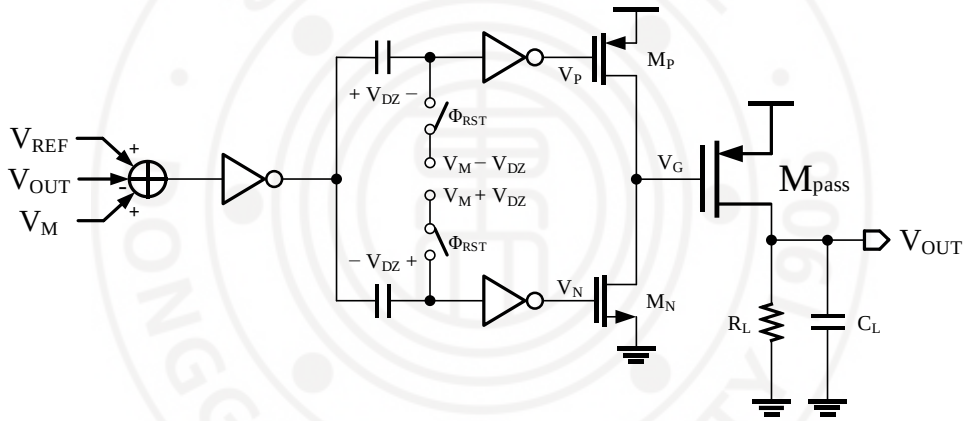
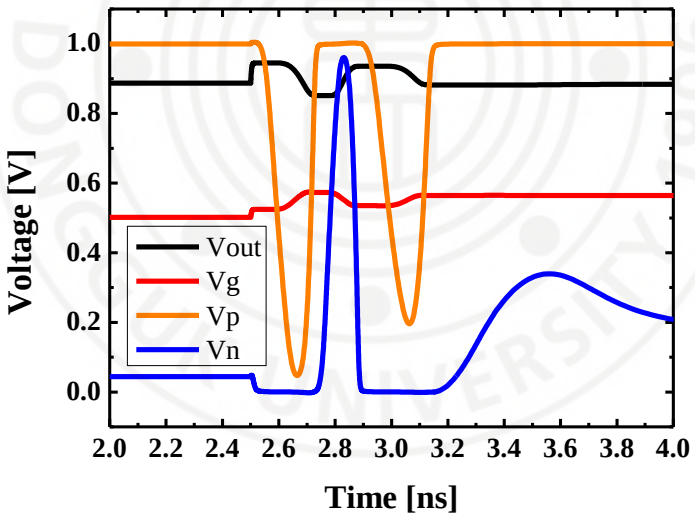


Figure 4.1-5 LDO with Fundamental Ring Amplifier.

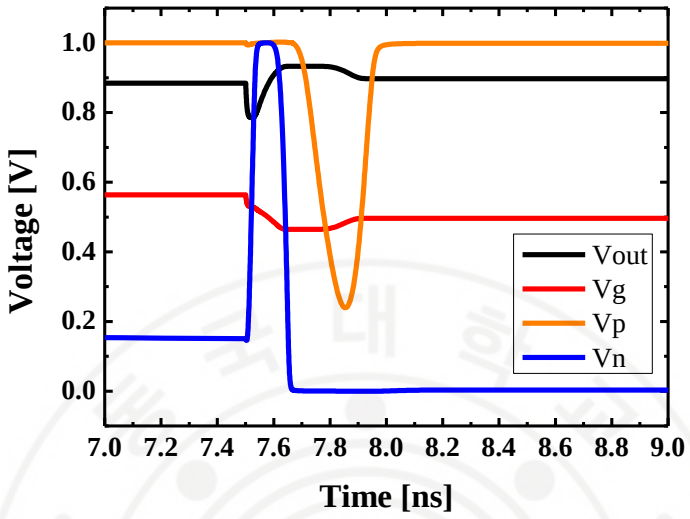
Simulation result for time-domain response of the LDO by a load step is shown in Figure 4.1-6. In Figure 4.1-6(a), the pass transistor charges C_L by a sudden decrease of load current. Then, the ring amplifier fully turns on the transistor M_P by the increase in V_{out}, which causes initial slewing of V_g and discharging of C_L. Initial slewing continues until V_{out} reaches dead-zone. The overshoot voltage is expressed as

$$V_{ovs} = -\frac{I_{RAMP}\tau_d}{C_g} g_m R_L. \quad (4.1\text{-}5)$$

similar to the switched-capacitor case, the effective output error is decreased by input-referred dead-zone voltage, V_{DZi}. Through the progressive decrease of slewing current during stabilization phase the LDO reaches steady-state.



(a)



(b)

Figure 4.1-6 Simulated transient response of Ring LDO. (a) is load step down and (b) is load step up situation.

The final error of the LDO follows (4.1-4). For dead-zone biasing of 200mV and voltage gain of first stage being 10V/V, the input referred dead-zone voltage is about 20mV. This means the output voltage of LDO could vary up to 40mV. This is often too large for most of applications. The operating speed of ring amplifier is very slow at steady state, which means the LDO can only reject supply ripple of low frequency or need another continuous-time signal path. The dead-zone bias is applied before second stage using capacitor. Reset phase is required to ensure proper operation. During reset phase, the feedback is disabled. While the class-B ringamp example demonstrated the prospect of scalable analog regulation, it required some modifications.

4.2 Ring LDO with Dynamic Cascode Bias

As we discussed earlier, using ring amplifier as an error amplifier of a LDO brought up several design objectives that have to be addressed. The ring amplifier should work with continuous-time signal with no dead-zone, consume small quiescent current, and get the most out of advantage of deeply scaled CMOS technology. Enabling sub-threshold operation can also improve the practicality as a regulator for digital systems. Using adaptive dead-zone ring amplifier[49] achieved continuous-time regulation along with adaptive bias to stabilize the LDO across wide load current range, but the transient response was not fast and lacked the information about PSRR and subthreshold operation. Replica-based PSR enhancement[50] demonstrated power supply rejection across wide frequency range and class-B ring amplifier path for transient response. Moreover, using time-interleaved auto-zeroing inverter made the LDO operate at wide range of supply voltage, even to sub-threshold region. The LDO separated signal path into main regulation path and class-B transient path. However, this resulted in a quiescent current up to 1.28mA at maximum power supply, degrading current efficiency.

The class-AB biasing is more suitable to reject power supply ripple over wide frequency. With class-AB biasing, the last stage of ring amplifier operates at sub-threshold region which is weak zone. By removing dead-zone, the amplifier continuously operates with reduced speed at steady-state. One way to realize it is self-biased ring amplifier[51]. Dynamic cascode bias can improve voltage gain

without compromising output slew current[52]. In this thesis, Ring LDO using class-AB dynamic cascode bias is proposed. Schematic diagram of proposed LDO is shown in Figure 4.2-1. Time-interleaved auto-zeroing switch enabled continuous-time regulation. Power cycling can reduce quiescent current by turning off the amplifier during reset phase. Replica-based PSR enhancement improved PSRR of the LDO. Applying MOS switch enabled sub-threshold operation of the LDO.

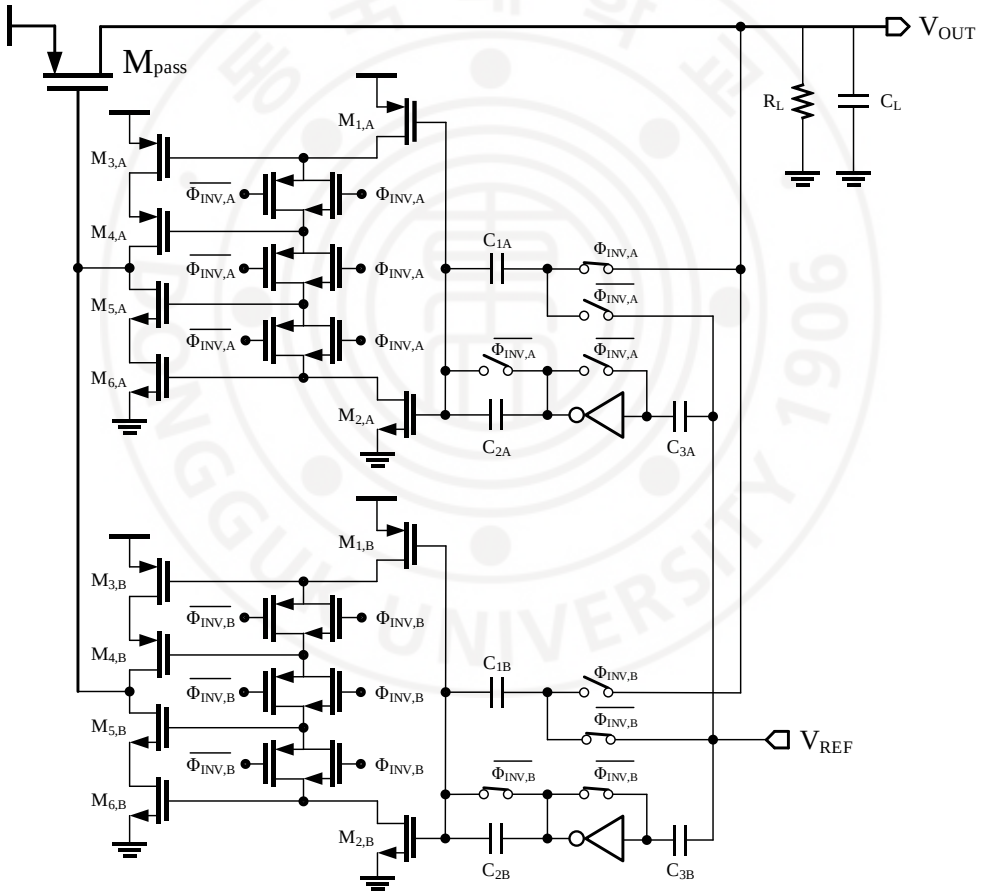


Figure 4.2-1 Schematic diagram of proposed LDO.

4.2.1 Dynamic Cascode Biasing

Dynamic cascode bias ring amplifier using MOS pseudo-resistor is shown in Figure 4.2-2. Using small switch can provide sufficient offset bias. In normal operation, transistors in second stage operate at sub-threshold due to reduced gate-source voltage with offset bias.

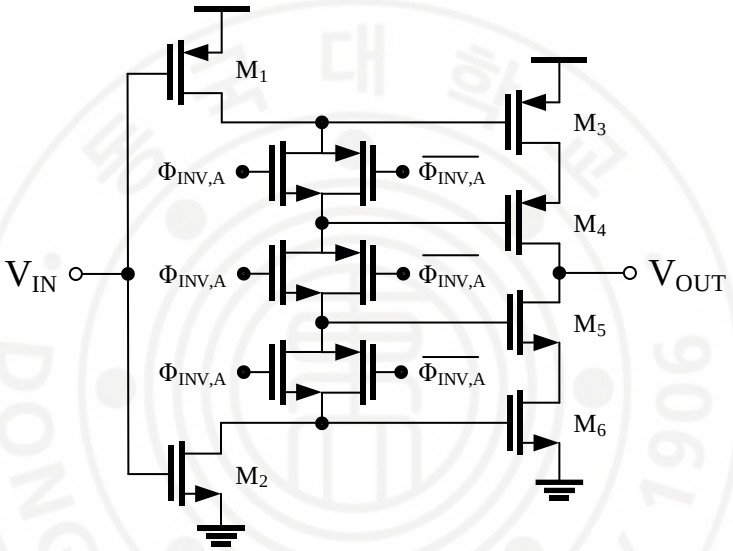


Figure 4.2-2 Schematic diagram of proposed ring amplifier.

Simulation result of short-circuit output current with respect to input voltage is shown in Figure 4.2-3. Through offset bias with MOS resistor, a weak-zone is formed. Input referred weak-zone voltage was 20mV. With input voltage larger than weak zone voltage, the effective transconductance and unity-gain bandwidth is dramatically increased. Periodic steady state (PSS) simulation result is shown in Figure 4.2-4. With input voltage of 1uVpk to 30mVpk, the short-circuit transconductance is increased from 187uS to 1.9mS, the unity-gain bandwidth is

increased from 26.9MHz to 378MHz. On the other hand, the voltage gain is reduced from 57.1dB to 33.5dB.

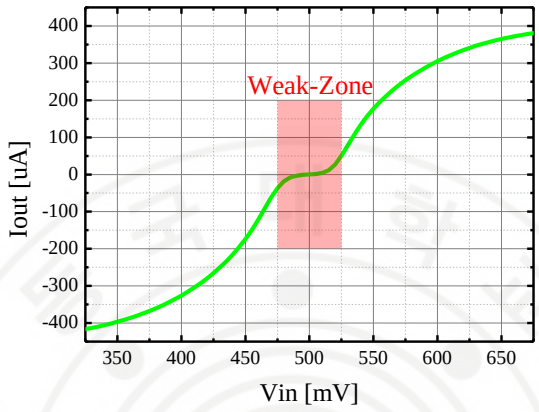
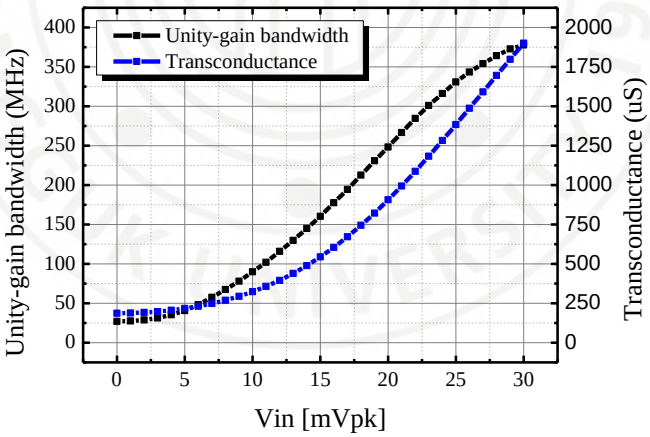
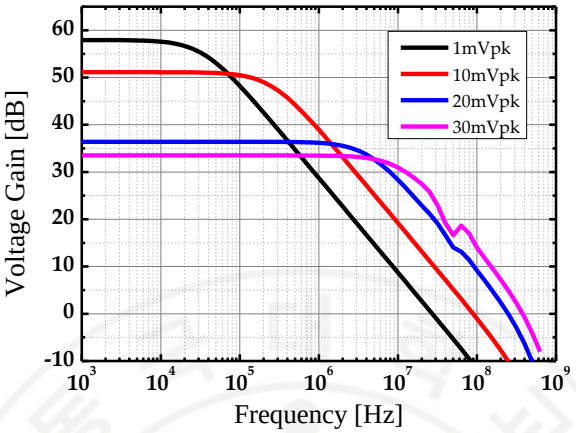


Figure 4.2-3 Simulation result of output current.



(a)



(b)

Figure 4.2-4 Periodic state state (PSS) simulation result.

4.2.2 Transient operation and Power Cycling

Transient simulation of a ring amplifier is shown in Figure 4.2-5 and Figure 4.2-6. When put in a feedback loop of LDO, The ring amplifier quickly responds to load transient step and sources/sinks current much larger than steady state current consumption. Once the output of LDO reaches desired value, the last stage of ring amplifier goes back to sub-threshold, stabilizing loop and enhancing accuracy. In reset phase, the MOS resistors are turned off and internal nodes are reset. The output of the amplifier is controlled by another ring amplifier. As a result, current consumption of time-interleaved ring amplifier almost equals that of single ring amplifier.

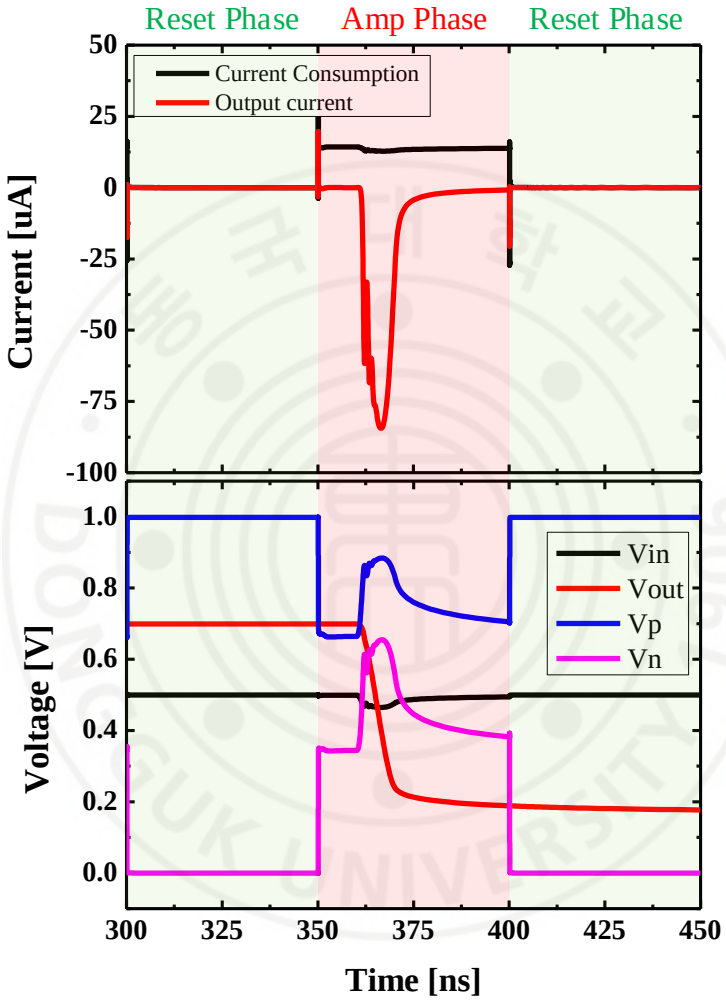


Figure 4.2-5 Transient simulation result of ring amplifier.

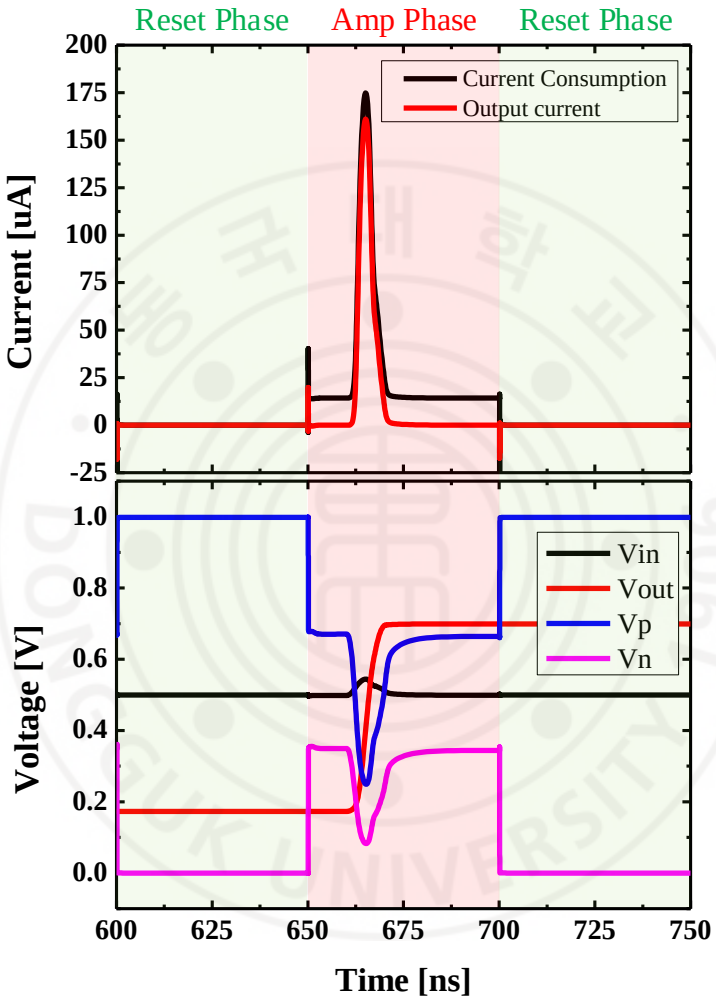


Figure 4.2-6 Transient simulation result of ring amplifier.

4.3 Simulation result

With Samsung 28nm CMOS technology, the circuit occupied active area of 0.0036mm^2. We performed simulation using commercial circuit simulator. The simulation included parasitic elements from layout effects.

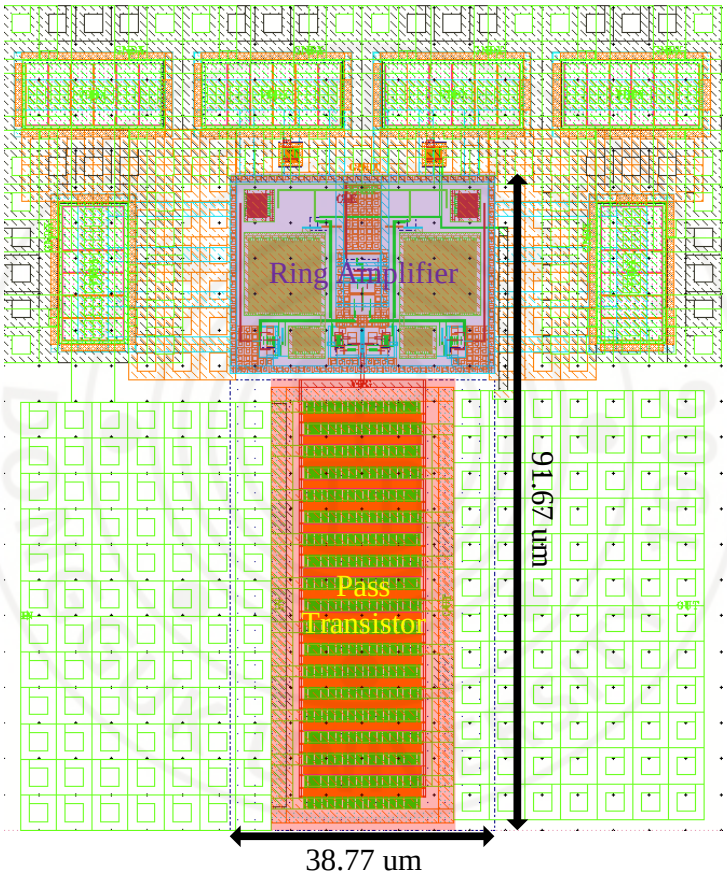


Figure 4.3-1 Layout of proposed ring LDO.

4.3.1 Power Supply Rejection Ratio (PSRR)

We performed power supply rejection ratio simulation with periodic ac simulator. With load current of 20mA and power supply voltage of 1V and dropout voltage of 100mV, the proposed LDO achieved PSRR of -58dB both with f_{clk}=100kHz and f_{clk}=1MHz.

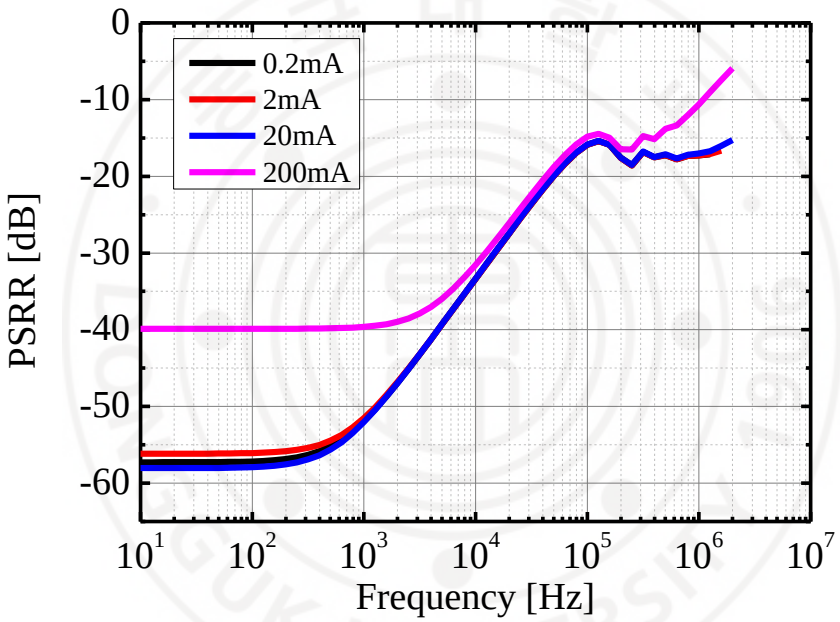


Figure 4.3-2 PSRR simulation result with f_{clk}=100kHz.

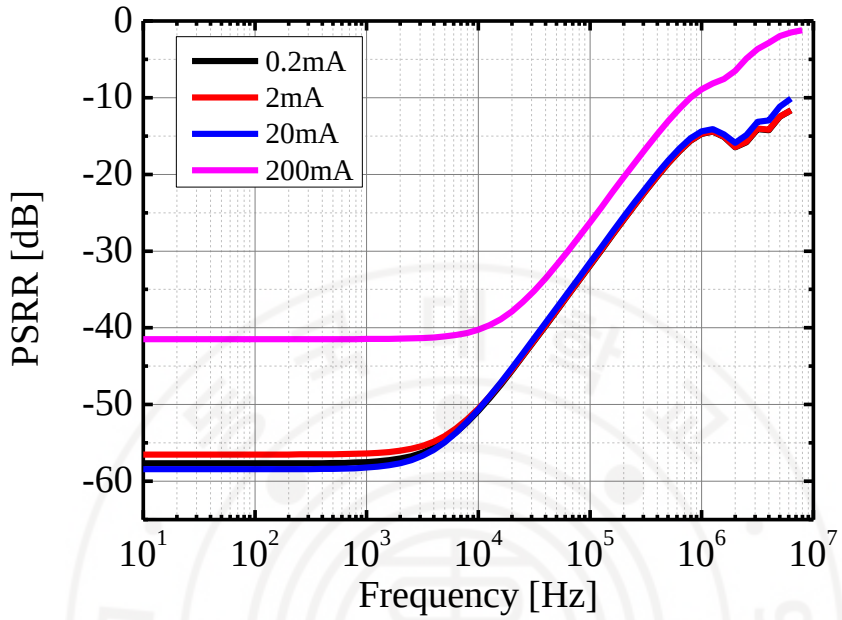


Figure 4.3-3 PSRR simulation result with f_{clk}=1MHz.

With auto-zeroing switch, the LDO is reset to appropriate amplifier DC input value. In addition, the on resistance of MOS is increased with low supply voltage. As a result, offset embedding with MOS resistor can track supply voltage variation better than normal resistor. With power supply voltage of 400mV, dropout voltage of 100mV and load current of 250uA, the proposed LDO achieved power supply rejection ratio of -30.86dB with f_{clk}=10kHz and -32.77dB with fclk=100kHz.

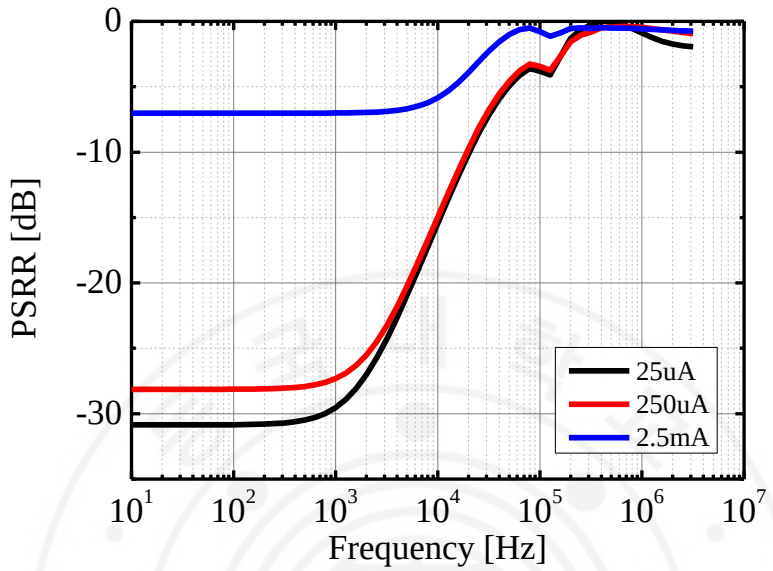


Figure 4.3-4 PSRR simulation result for sub-threshold with fclk=10kHz.

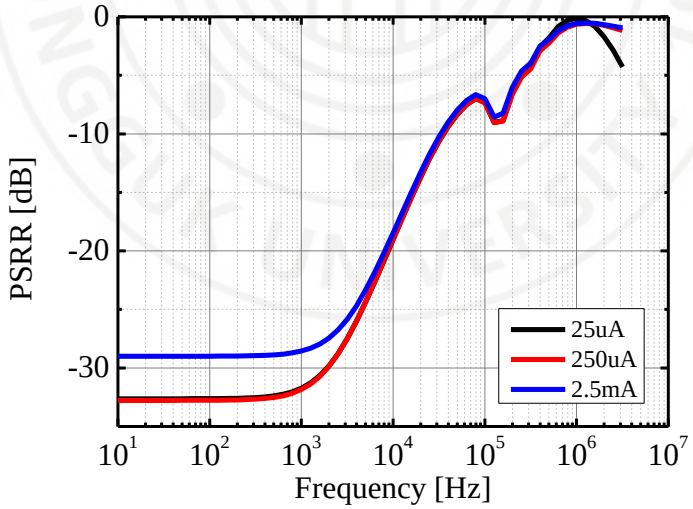


Figure 4.3-5 PSRR simulation result for sub-threshold with flck=100kHz.

4.3.2 Transient Response

We performed transient simulation with load step. Simulation result with supply voltage of 1V, dropout voltage of 100mV and f_{clk}=100MHz is shown in Figure 4.3-6. The output voltage varied up to 77mV by a load step from 2mA to 200mA within 5ns. The quiescent current was 42.4uA. Response time and transient figure-of-merit calculated by (3.3-1) and (3.3-2) was 197ps and 41.8fs, respectively. The LDO settled to final value within 28ns.

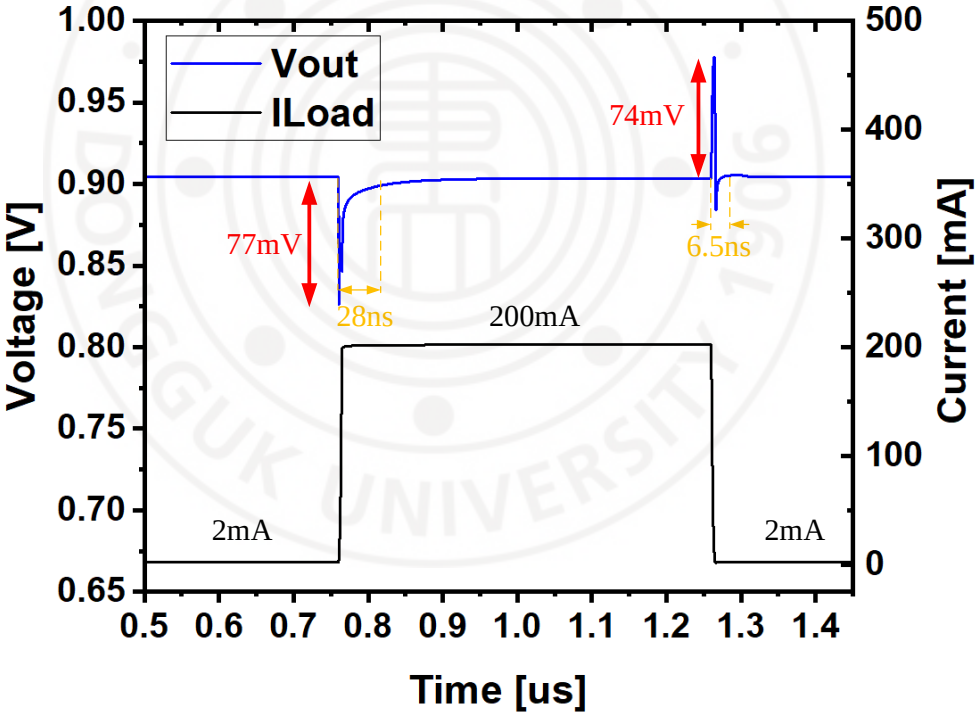


Figure 4.3-6 Transient simulation result.

Simulation result with supply voltage of 0.4V, dropout voltage of 100mV and fclk=100kHz is shown in Figure 4.3-7. The output voltage varied up to 164mV by a load step from 25uA to 2.5mA within 5ns. The quiescent current was 101nA. Response time and transient figure-of-merit calculated by (3.3-1) and (3.3-2) was 1.2081ns and 48.8fs, respectively. The LDO settled to final value within 590ns

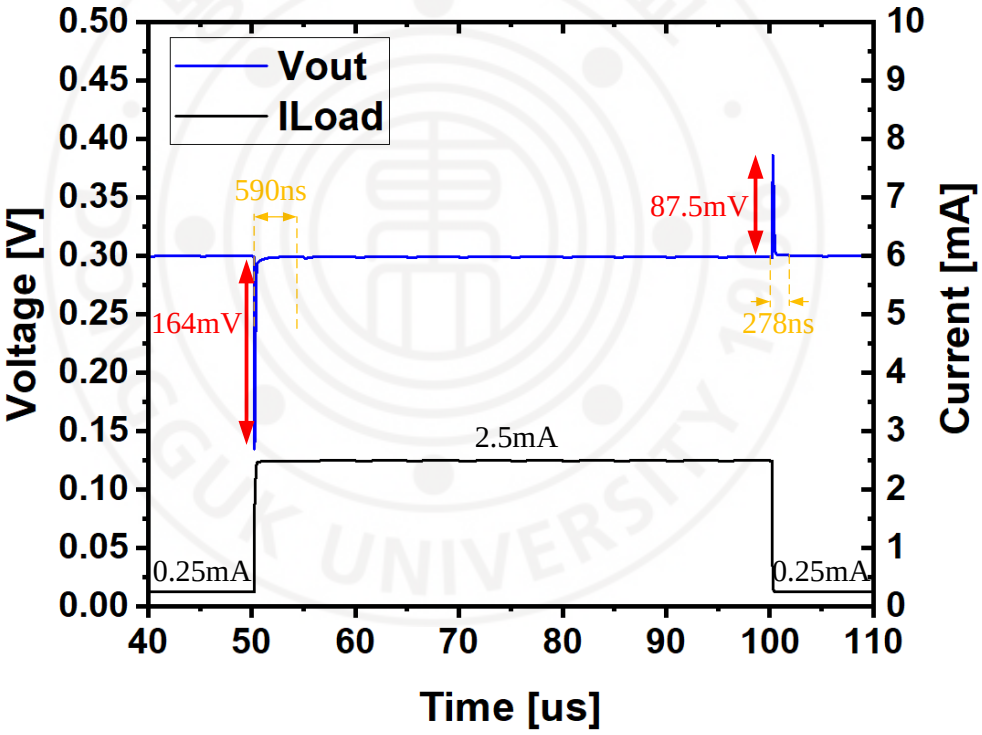


Figure 4.3-7 Transient simulation result with subthreshold operation.

4.3.3 Discussion

Table 4.3-1 summarizes the performance of the proposed Ring LDO with other state-of-the-art LDOs. The proposed Ring LDO occupied a 0.0036 mm^2 active area. The LDO output was from 0.3V to 1.1V with supply voltage from 0.4V to 1.2V. The maximum output current was 200mA, and the quiescent current at 1V supply was 42.4uA. And output capacitor of 10pF was used, occupying very less area. The proposed LDO could handle large current for less area. The current density was 56275mA/mm2, which was second in the table. The proposed LDO achieved better PSRR and faster load regulation than digital LDO. It achieved best response time of 0.197ns and 41.8fs transient figure-of-merit, yet consuming 10x less current than previous ring LDO implementation. Computational digital LDO achieved very fast transient response with large current step at the expense of consuming staggering 2.4mA, which was less dependent to load current. The proposed ring LDO also can vastly improve PSRR. While many digital LDOs have shown unsatisfactory PSRR or have not proven PSRR performance, the PSRR of proposed ring LDO could reach −50 dB at 10kHz. In general, the ring amplifier with dynamic cascode bias could achieve fast and accurate regulation with less current consumption. In future research, advanced switching mechanism could be applied to reduce clock feedthrough. Integrated clock generator could also be included to reduce system complexity of power management IC.

Table 4.3-1 Performance comparison between state-of-the-art LDOs.

LDO	This Work†	[50]	[53]	[31]
Type	Analog (Ring)	Analog (Ring)	Digital (Coarse-fine)	Digital (Computational)
Process [nm]	28	40	28	22
Area [mm^2]	0.0036	0.0057	0.021	0.165
V_{in} [V]	0.4-1.2	0.4-1.2	1.1	0.55-1.2
V_{out} [V]	0.3-1.1	0.2-1.18	0.9	0.5-1.15
I_Q [uA]	0.1-119	4.4-1280	110	2400
Max. I_{load} [mA]	200	400	200	2000
Current Density [mA/mm^2]	56275	70175	9524	12121
Load capacitor [nF]	0.01	0.09	23.5	7
Load transient Overshoot [mV]	77 @5ns step	45 @10ns step	200 @4us step	100 @0.25ns step
Settling Time @Max. current step [ns]	28	25	40000*	15
T_R [ns]	0.197	0.636	457	0.79
Transient FoM [ps]	0.0418	0.864	251.3	0.948
PSRR [dB]	-50.6@10kHz -14.3@1MHz	-34@10kHz -25 @1MHz	-	-
Load regulation [uV/mA]	5.03	50*	-	-

* Estimated from figure. †Simulated.

Chapter 5 Conclusion

This thesis demonstrated LDO design approach for analog and digital electronic systems. A direct feedback flipped voltage follower LDO is proposed as a suitable LDO design for analog circuits. Such simple structure is easier to design, and improved power supply rejection of LDO while not sacrificing transient response. Stability and parameter variation sensitivity analysis of FVF LDO through state matrix decomposition is also presented. The LDO is fabricated with TSMC 65nm CMOS technology. The fabricated FVF LDO supplies maximum load current of 20mA with 1.2V power supply. Proposed FVF LDO achieves full-spectrum PSR with low-frequency PSRR of 66 dB, unity-gain bandwidth of 416MHz, 20ns transient settling time with load current step from 1mA to 20mA. A ring LDO with dynamic cascode biasing is proposed as a suitable LDO design for digital circuits. Class-AB ring amplifier enables continuous-time regulation along with accurate steady-state output. Compact amplifier comprising simple digital elements enabled area-efficient implementation. The proposed ring LDO achieved transient response time of 0.197ns and 41.8fs transient FoM and 50.6dB PSRR at 10kHz.

For the future research, current-mode feed-forward ripple cancellation may improve PSRR of FVF LDO over wide range of frequency. Ring amplifier with adaptive bias can be also studied to improve stable current range of ring LDO.

REFERENCES

[1] T. Coulot, E. Lauga-Larroze, J.-M. Fournier, M. Alamir, and F. Hasbani, "Stability Analysis and Design Procedure of Multiloop Linear LDO Regulators via State Matrix Decomposition," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5352–5363, Nov. 2013, doi: 10.1109/TPEL.2013.2241456.

[2] K.-W. Ha, J.-Y. Lee, G.-H. Ko, Y.-J. Kim, J.-G. Kim, and D. Baek, "Fully Integrated Dual-Mode X-Band Radar Transceiver Using Configurable Receiver and Local Oscillator," *IEEE Access*, vol. 8, pp. 151403–151414, 2020, doi: 10.1109/ACCESS.2020.3016689.

[3] T. Ma *et al.*, "A CMOS 76–81-GHz 2-TX 3-RX FMCW Radar Transceiver Based on Mixed-Mode PLL Chirp Generator," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 233–248, Feb. 2020, doi: 10.1109/JSSC.2019.2950184.

[4] J. K. Ha *et al.*, "RF Transceiver for the Multi-Mode Radar Applications," *Sensors*, vol. 21, no. 5, p. 1563, Feb. 2021, doi: 10.3390/s21051563.

[5] K.-W. Ha, J.-Y. Lee, J.-G. Kim, and D. Baek, "Design of Dual-Mode Local Oscillators Using CMOS Technology for Motion Detection Sensors," *Sensors*, vol. 18, no. 4, p. 1057, Apr. 2018, doi: 10.3390/s18041057.

[6] D. Saunders *et al.*, "A single-chip 24 GHz SiGe BiCMOS transceiver for FMCW automotive radars," in *2009 IEEE Radio Frequency Integrated Circuits Symposium*, Boston, MA, USA, Jun. 2009, pp. 459–462. doi: 10.1109/RFIC.2009.5135580.

[7] J. Chen, W. Zhang, Q. Sun, and L. Liu, "An 8–12.5-GHz LC PLL with Dual VCO and Noise-Reduced LDO Regulator for Multilane Multiprotocol SerDes in 28-nm CMOS Technology," *Electronics*, vol. 10, no. 14, Art. no. 14, Jan. 2021, doi: 10.3390/electronics10141686.

[8] A. Arakali, S. Gondi, and P. K. Hanumolu, "Analysis and Design Techniques for Supply-Noise Mitigation in Phase-Locked Loops," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 11, pp. 2880–2889, Nov. 2010, doi: 10.1109/TCSI.2010.2052507.

[9] Chang-Hyeon Lee, K. McClellan, and J. Choma, "A supply-noise-insensitive CMOS PLL with a voltage regulator using DC-DC capacitive converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1453–1463, Oct. 2001, doi: 10.1109/4.953473.

[10] H. C. Ngo, K. Nakata, T. Yoshioka, Y. Terashima, K. Okada, and A. Matsuzawa, "8.5 A 0.42ps-jitter −241.7dB-FOM synthesizable injection-locked PLL with noise-isolation LDO," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, Feb. 2017, pp. 150–151. doi: 10.1109/ISSCC.2017.7870305.

[11] L. Wang, W. Mao, C. Wu, A. Chang, and Y. Lian, "A fast transient LDO based

on dual loop FVF with high PSRR," in *2016 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Jeju, South Korea, Oct. 2016, pp. 99–102. doi: 10.1109/APCCAS.2016.7803906.

[12] V.-S. Trinh, H. Nam, J.-M. Song, and J.-D. Park, "A 78.8–84 GHz Phase Locked Loop Synthesizer for a W-Band Frequency-Hopping FMCW Radar Transceiver in 65 nm CMOS," *Sensors*, vol. 22, no. 10, p. 3626, May 2022, doi: 10.3390/s22103626.

[13] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sanchez-Sinencio, "High PSR Low Drop-Out Regulator With Feed-Forward Ripple Cancellation Technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 565–577, Mar. 2010, doi: 10.1109/JSSC.2009.2039685.

[14] Y.-J. Choe, H. Nam, and J.-D. Park, "A Low-Dropout Regulator with PSRR Enhancement through Feed-Forward Ripple Cancellation Technique in 65 nm CMOS Process," *Electronics*, vol. 9, no. 1, p. 146, Jan. 2020, doi: 10.3390/electronics9010146.

[15] K. Joshi, S. Manandhar, and B. Bakkaloglu, "A 5.6 μ A Wide Bandwidth, High Power Supply Rejection Linear Low-Dropout Regulator With 68 dB of PSR Up To 2 MHz," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 8, pp. 2151–2160, Aug. 2020, doi: 10.1109/JSSC.2020.2978033.

[16] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sanchez-Sinencio, "A 25mA 0.13μm CMOS LDO regulator with power-supply rejection better than −56dB up to 10MHz using a feedforward ripple-cancellation technique," in *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb. 2009, pp. 330-331,331a. doi: 10.1109/ISSCC.2009.4977442.

[17] Y. Lim, J. Lee, S. Park, Y. Jo, and J. Choi, "An External Capacitorless Low-Dropout Regulator With High PSR at All Frequencies From 10 kHz to 1 GHz Using an Adaptive Supply-Ripple Cancellation Technique," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2675–2685, Sep. 2018, doi: 10.1109/JSSC.2018.2841984.

[18] D.-K. Kim, S.-U. Shin, and H.-S. Kim, "A BGR-Recursive Low-Dropout Regulator Achieving High PSR in the Low- to Mid-Frequency Range," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13441–13454, Dec. 2020, doi: 10.1109/TPEL.2020.2996771.

[19] Y.-P. Chen and K.-T. Tang, "A Fully Integrated High-Power-Supply-Rejection Linear Regulator With an Output-Supplied Voltage Reference," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 11, pp. 3828–3838, Jan. 2020, doi: 10.1109/TCSI.2020.3008031.

[20] C. Răducan, M. Neag, A. Grăjdeanu, M. Țopa, and A. Negoiță, "High-Precision Low-Temperature Drift LDO Regulator Tailored for Time-Domain Temperature Sensors," *Sensors*, vol. 22, no. 4, Art. no. 4, Jan. 2022, doi: 10.3390/s22041518.

[21] S.-W. Hong and G.-H. Cho, “High-Gain Wide-Bandwidth Capacitor-Less Low-Dropout Regulator (LDO) for Mobile Applications Utilizing Frequency Response of Multiple Feedback Loops,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 1, pp. 46–57, Jan. 2016, doi: 10.1109/TCSI.2015.2512702.

[22] K. Li, C. Yang, T. Guo, and Y. Zheng, “A Multi-Loop Slew-Rate-Enhanced NMOS LDO Handling 1-A-Load-Current Step With Fast Transient for 5G Applications,” *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 3076–3086, Nov. 2020, doi: 10.1109/JSSC.2020.3005789.

[23] Y. Jiang, L. Wang, Y. Wang, S. Wang, and M. Guo, “A High-Loop-Gain Low-Dropout Regulator with Adaptive Positive Feedback Compensation Handling 1-A Load Current,” *Electronics*, vol. 11, no. 6, Art. no. 6, Jan. 2022, doi: 10.3390/electronics11060949.

[24] W. Oh and B. Bakkaloglu, “A CMOS Low-Dropout Regulator With Current-Mode Feedback Buffer Amplifier,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 10, pp. 922–926, Oct. 2007, doi: 10.1109/TCSII.2007.901621.

[25] B. H. Calhoun and A. P. Chandrakasan, “Ultra-Dynamic Voltage Scaling (UDVS) Using Sub-Threshold Operation and Local Voltage Dithering,” *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 238–245, Jan. 2006, doi: 10.1109/JSSC.2005.859886.

[26] E. J. Fluhr *et al.*, “The 12-Core POWER8™ Processor With 7.6 Tb/s IO Bandwidth, Integrated Voltage Regulation, and Resonant Clocking,” *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 10–23, Jan. 2015, doi: 10.1109/JSSC.2014.2358553.

[27] R. Muthukaruppan *et al.*, “A digitally controlled linear regulator for per-core wide-range DVFS of atom™ cores in 14nm tri-gate CMOS featuring non-linear control, adaptive gain and code roaming,” in *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, Leuven, Sep. 2017, pp. 275–278. doi: 10.1109/ESSCIRC.2017.8094579.

[28] C. Gonzalez *et al.*, “The 24-Core POWER9 Processor With Adaptive Clocking, 25-Gb/s Accelerator Links, and 16-Gb/s PCIe Gen4,” *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 91–101, Jan. 2018, doi: 10.1109/JSSC.2017.2748623.

[29] Y.-H. Lee *et al.*, “A Low Quiescent Current Asynchronous Digital-LDO With PLL-Modulated Fast-DVS Power Management in 40 nm SoC for MIPS Performance Improvement,” *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1018–1030, Apr. 2013, doi: 10.1109/JSSC.2013.2237991.

[30] J. Oh, J.-E. Park, Y.-H. Hwang, and D.-K. Jeong, “25.2 A 480mA Output-Capacitor-Free Synthesizable Digital LDO Using CMP- Triggered Oscillator and Droop Detector with 99.99% Current Efficiency, 1.3ns Response Time,

and 9.8A/mm ^{2} Current Density," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, Feb. 2020, pp. 382–384. doi: 10.1109/ISSCC19947.2020.9063018.

[31] Z. K. Ahmed *et al.*, "A Variation-Adaptive Integrated Computational Digital LDO in 22nm CMOS with Fast Transient Response," in *2019 Symposium on VLSI Circuits*, Kyoto, Japan, Jun. 2019, pp. C124–C125. doi: 10.23919/VLSIC.2019.8778070.

[32] Tsz Yin Man, Ka Nang Leung, Chi Yat Leung, P. K. T. Mok, and Mansun Chan, "Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 5, pp. 1392–1401, Jun. 2008, doi: 10.1109/TCSI.2008.916568.

[33] Y. Lu, W.-H. Ki, and C. P. Yue, "17.11 A 0.65ns-response-time 3.01ps FOM fully-integrated low-dropout regulator with full-spectrum power-supply-rejection for wideband communication systems," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, San Francisco, CA, USA, Feb. 2014, pp. 306–307. doi: 10.1109/ISSCC.2014.6757446.

[34] G. Cai, Y. Lu, C. Zhan, and R. P. Martins, "A Fully Integrated FVF LDO With Enhanced Full-Spectrum Power Supply Rejection," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4326–4337, Apr. 2021, doi: 10.1109/TPEL.2020.3024595.

[35] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, Apr. 2005, doi: 10.1109/JSSC.2004.842831.

[36] S. Bu, J. Guo, and K. N. Leung, "A 200-ps-Response-Time Output-Capacitorless Low-Dropout Regulator With Unity-Gain Bandwidth >100 MHz in 130-nm CMOS," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3232–3246, Apr. 2018, doi: 10.1109/TPEL.2017.2711017.

[37] D. Kim and M. Seok, "8.2 Fully integrated low-drop-out regulator based on event-driven PI control," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, Jan. 2016, pp. 148–149. doi: 10.1109/ISSCC.2016.7417950.

[38] S. J. Kim, D. Kim, H. Ham, J. Kim, and M. Seok, "A 67.1-ps FOM, 0.5-V-Hybrid Digital LDO With Asynchronous Feedforward Control Via Slope Detection and Synchronous PI With State-Based Hysteresis Clock Switching," *IEEE Solid-State Circuits Letters*, vol. 1, no. 5, pp. 130–133, May 2018, doi: 10.1109/LSSC.2018.2875828.

[39] J.-E. Park and D.-K. Jeong, "A Fully Integrated 700mA Event-Driven Digital Low-Dropout Regulator with Residue-Tracking Loop for Fine-Grained Power Management Unit," in *2018 IEEE Symposium on VLSI Circuits*, Honolulu, HI,

Jun. 2018, pp. 231–232. doi: 10.1109/VLSIC.2018.8502295.
[40] X. Sun, A. Boora, W. Zhang, V. R. Pamula, and V. Sathe, "14.5 A 0.6-to-1.1V Computationally Regulated Digital LDO with 2.79-Cycle Mean Settling Time and Autonomous Runtime Gain Tracking in 65nm CMOS," in *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, Feb. 2019, pp. 230–232. doi: 10.1109/ISSCC.2019.8662298.
[41] B. H. Calhoun and A. Chandrakasan, "Characterizing and modeling minimum energy operation for subthreshold circuits," in *Proceedings of the 2004 International Symposium on Low Power Electronics and Design (IEEE Cat. No.04TH8758)*, Aug. 2004, pp. 90–95. doi: 10.1145/1013235.1013265.
[42] M. Liu, X. Zhang, H. Chen, C. Zhang, and Z. Wang, "A fast computable delay model for subthreshold circuit," in *2012 25th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, Apr. 2012, pp. 1–4. doi: 10.1109/CCECE.2012.6334918.
[43] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, and U.-K. Moon, "Ring amplifiers for switched-capacitor circuits," in *2012 IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, Feb. 2012, pp. 460–462. doi: 10.1109/ISSCC.2012.6177090.
[44] J. Lagos, B. P. Hershberg, E. Martens, P. Wambacq, and J. Craninckx, "A 1-GS/s, 12-b, Single-Channel Pipelined ADC With Dead-Zone-Degenerated Ring Amplifiers," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 646–658, Mar. 2019, doi: 10.1109/JSSC.2018.2889680.
[45] Y. Lim and M. P. Flynn, "A 1 mW 71.5 dB SNDR 50 MS/s 13 bit Fully Differential Ring Amplifier Based SAR-Assisted Pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2901–2911, Dec. 2015, doi: 10.1109/JSSC.2015.2463094.
[46] S. Leuenberger, J. Muhlestein, H. Sun, P. Venkatachala, and U.-K. Moon, "A 74.33 dB SNDR 20 MSPS 2.74 mW pipelined ADC using a dynamic deadzone ring amplifier," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, Apr. 2017, pp. 1–4. doi: 10.1109/CICC.2017.7993697.
[47] T.-C. Hung and T.-H. Kuo, "A 75.3-dB SNDR 24-MS/s Ring Amplifier-Based Pipelined ADC Using Averaging Correlated Level Shifting and Reference Swapping for Reducing Errors From Finite Opamp Gain and Capacitor Mismatch," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1425–1435, May 2019, doi: 10.1109/JSSC.2019.2891650.
[48] B. Hershberg *et al.*, "3.1 A 3.2GS/s 10 ENOB 61mW Ringamp ADC in 16nm with Background Monitoring of Distortion," in *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, Feb. 2019, pp. 58–60. doi: 10.1109/ISSCC.2019.8662290.
[49] B. Xiao *et al.*, "An 80mA Capacitor-Less LDO with 6.5µA Quiescent Current and No Frequency Compensation Using Adaptive-Deadzone Ring Amplifier,"

in *2019 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Macau, Macao, Nov. 2019, pp. 39–42. doi: 10.1109/A-SSCC47793.2019.9056970.

[50] J.-E. Park, J. Hwang, J. Oh, and D.-K. Jeong, "32.4 A 0.4-to-1.2V 0.0057mm ^{2} 55fs-Transient-FoM Ring-Amplifier-Based Low-Dropout Regulator with Replica-Based PSR Enhancement," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, Feb. 2020, pp. 492–494. doi: 10.1109/ISSCC19947.2020.9063147.

[51] Y. Lim and M. P. Flynn, "A 100 MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2331–2341, Oct. 2015, doi: 10.1109/JSSC.2015.2453332.

[52] C. Y. Lee, P. K. Venkatachala, A. ElShater, B. Xiao, H. Hu, and U.-K. Moon, "Cascoded Ring Amplifiers for High Speed and High Accuracy Settling," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, May 2019, pp. 1–5. doi: 10.1109/ISCAS.2019.8702710.

[53] Y.-J. Lee *et al.*, "A 200-mA Digital Low Drop-Out Regulator With Coarse-Fine Dual Loop in Mobile Application Processor," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 64–76, Jan. 2017, doi: 10.1109/JSSC.2016.2614308.

국문 초록

본 연구는 아날로그 시스템에 적용 가능한 FVF 저 드롭아웃 전압 레귤레이터(Low-Dropout Regulator, LDO)와 디지털 시스템에 적용 가능한 링 LDO 구조를 제안한다. 아날로그 시스템용 전압 레귤레이터 사양을 만족하기 위해 TSMC 65nm CMOS 공정으로 이중 루프를 사용하는 FVF(Flipped Voltage Follower) LDO를 설계 및 제작하였다. 제안된 FVF LDO는 높은 전원 리플 제거(PSR)를 위한 저속 루프와 고주파 전원 리플 제거를 위한 고속 루프로 구성되어 효과적으로 넓은 대역의 전원 리플을 제거한다. 고속 루프에는 패스 트랜지스터 구동을 위해 super source follower를 사용하여 적은 전력 소모로 루프 작동 속도를 향상시켰다. 상태 행렬 분해 기법(State Matrix Decomposition Method)을 사용하여 매개변수 변동에 따른 다중 루프 LDO의 안정성을 평가하였고 시뮬레이션 결과와 일치함을 확인하였다. 구현된 FVF LDO는 unity gain frequency 400MHz, 저주파 PSRR 66dB, 1.2V-1.6V 입력 전압 범위 안에서 1.04uV/mV의 Line regulation, 출력 전류 범위 2mA-20mA에서 안정적으로 작동하였다. 디지털 시스템용 전압 레귤레이터 사양을 만족하기 위해 삼성 28nm CMOS 공정으로 링 LDO를 설계 및 제작하였다. 루프 작동 속도를 유지하면서 대기 전류를 줄이기 위해 동적 바이어스 캐스코드 링

증폭기를 사용하였다. 캐스코드 구조가 포함되어 폐쇄 루프 이득이 향상되었고 디지털 LDO에 비해 PSRR이 비약적으로 향상되었다. 구현된 Ring LDO 는 0.4V-1.2V 입력 전압 범위, 55000mA/um2의 출력 전류 밀도를 가지며 부하 계단 응답에서 최대 28ns의 정착 시간을 달성하였다. 제안된 링 LDO는 미세공정에서도 스케일 가능한 링 증폭기를 사용하여 디지털 시스템용 전집적화된 전압 레귤레이터에 적합하며 단순한 논리 게이트와 캐패시터로 구성되므로 적은 면적으로 실현 가능하다.