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Thesis for the Degree of Master of Engineering

Ultra-Wideband Driver Design for 200Gb/s Mach-Zehnder Modulator in SiGe Technology

Advisor: Professor Jung-Dong Park

Graduate School of Dongguk University
Department of Electronic and Electrical Engineering

Hyeong-Geun Park

2023

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by

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Date of submission : 2023/06

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Graduate School of Dongguk University

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Hyeong-geun Park

ABSTRACT

This thesis presents the ultra-wideband driver for Mach-Zehnder modulator (MZM) using 200 Gb/s PAM-4 (4 Level Pulse Amplitude Modulation) signal. The proposed driver, aimed at realizing next-generation high-speed optical networks, is composed of two distributed amplifiers (DA), a Wilkinson power divider, and a delay line for synchronizing the electrical and optical signals for modulation. The degenerated cascode topology is used at each unit cell to minimize distortion. Also, a tunable RC network utilized in the emitter degeneration to drive a 200 Gb/s PAM-4 signal at segmented-MZM electrode and improve the fidelity of the Eye Diagram. The RC network was designed to control the effective capacitance and resistance values by connecting the control bits to the gate of the MOS switch through an SPI (Serial Peripheral Interface) Scan-chain.

DA1 and DA2 of the designed driver were designed with 7 and 8 stages, respectively, to compensate for the insertion loss caused by the delay line. The designed driver achieved a 3dB gain bandwidth of 100 kHz-105 GHz, a small signal gain of over 9 dB at 70 GHz, and a saturated output power of 18 dBm at 70 GHz. The power consumption of the designed driver was 2.86W, and the chip size was 2.76 mm^2. When a PAM-4 signal of 100GBaud was input to the designed driver with 1Vppd, the output voltage magnitude of the driver met 3Vppd, and the Eye linearity and Eye skew in the output signal's Eye Diagram were 1 and 0, respectively. The

synchronization between the electrical signal input to MZM2's electrode and the optical signal passing through MZM1 and optical waveguide was realized.

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Chapter 1 Introduction

1.1 Research Background

As data traffic continually increases, the demand on the network infrastructure is becoming increasingly strained. By using optical formats such as the Mach-Zehnder Modulator (MZM), data can be sent with low power consumption and minimal loss over long distances. To transmit narrow pulses with fine spatial resolution, a wideband power amplifier is required to realize such a system [1].

In order to commercialize a silicon photonics optical transmitter, an integrated high-speed driver IC electronic device is essential. The driver should secure that can be connected to a silicon photonics-based MZM and can provide wide bandwidth performance and high voltage swing.

In this thesis, design considerations of ultra-wideband driver for separated MZM is investigated. We designed an ultra-wideband distributed amplifier (DA) for driving segmented traveling wave MZM's electrode to verify the purpose. The implemented chip includes "DA1 + DA2 with delay line", which is designed to achieve enough gain of PAM-4 signal with differential output for 200 Gb/s applications.

1.2 Thesis Organization

In Chapter 2, basic information about optical communication systems is introduced. Digital signaling, electro-optical modulation schemes, and MZM are explained in order to accomplish this. Chapter 3 presents the design method for standalone DA and discusses the design of the tuning network in the unit cell of the DA. Additionally, the synchronization of the designed DAs with the matched control of the Mach-Zehnder modulator (MZM) and elements design for synchronization is presented. Also, small signal and large signal measurement setups for each frequency are introduced. The simulation and layout of the designed DA were performed with Cadence Virtuoso. For the transmission line modeling, HFSS 3D EM simulation is used. Chapter 4 concludes the thesis and suggests future research directions.

Chapter 2 PAM-4 signal Optical modulation

2.1 Digital Signaling Scheme

There is a growing demand for higher data transfer rates in communication systems. Currently, non-return to zero (NRZ) signaling with 2 levels and one bit per level is widely used. However, in order to achieve even higher data transfer rates, the development of 4 level pulse amplitude modulation (PAM-4) has been introduced [2]. PAM-4 utilizes signaling with 4 levels and two bits per level. By employing PAM-4 modulation, communication systems can effectively double their data throughput without doubling of their bandwidth. This is due to the improved bandwidth efficiency of PAM-4 modulation [3].

2.1.1 Non-return to zero

The NRZ, also known as 2 level pulse amplitude modulation (PAM-2), is now a common standard for communication system. Figure 2.1-1 shows NRZ signaling. High or positive levels represent logic 1 and low or negative levels represent logic 0.

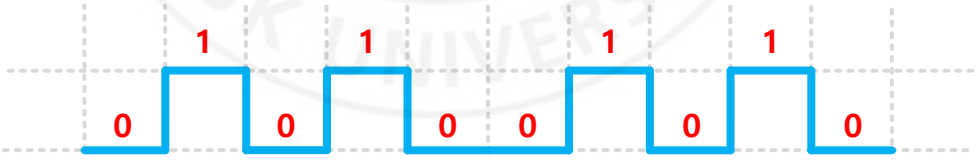


Figure 2.1-1 NRZ signaling

As shown in the Figure 2.1-2, NRZ generates 2 level signals with 1 eye opening. NRZ has 1 rising edge and 1 falling edge which makes 2 transition.

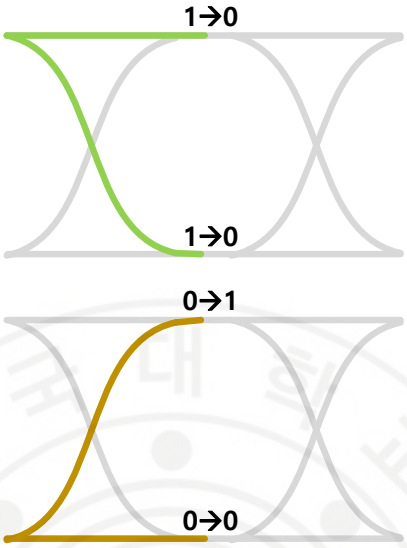


Figure 2.1-2 NRZ voltage logic levels

2.1.2 4 level pulse amplitude modulation (PAM-4)

Next generation signaling scheme is derived from NRZ by mapping the signal to four levels is called 4 level pulse amplitude modulation (PAM-4). As a solution to the NRZ limitations, PAM-4 is the evolution of data signaling format. Instead of two levels (0, 1) of modulation as in NRZ, PAM-4 uses four logic levels (00, 01, 11, 10) and every 2 bits corresponds to one voltage level. Figure 2.1-3 shows the PAM-4 signaling. PAM4 is generated with the sum of MSB and LSB which has amplitude of half of the MSB amplitude.

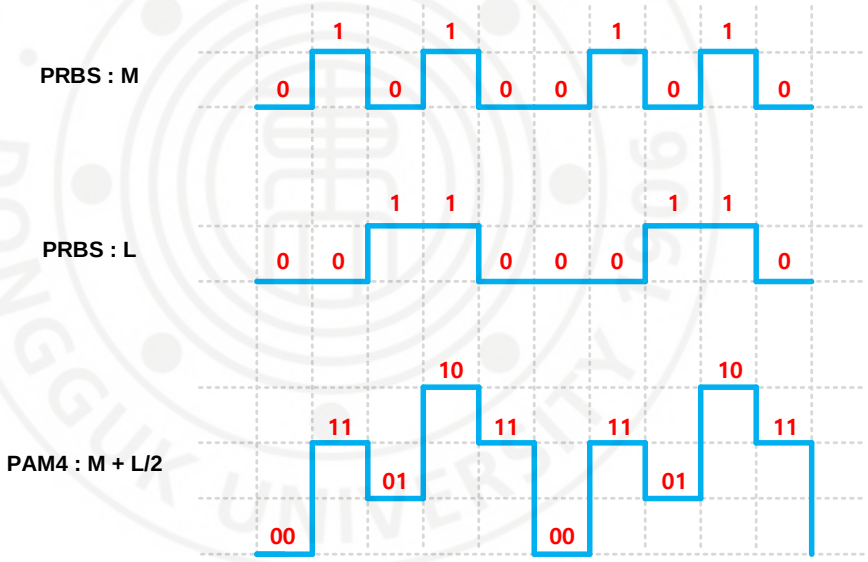


Figure 2.1-3 PAM-4 signaling

As shown in the Figure 2.1-4, PAM-4 generates 4 level signals with 3 eye openings. NRZ only has 1 rising edge and 1 falling edge which makes it 2 transition but in PAM-4 there are 6 rising edge and 6 falling edges that results in 12 transitions.

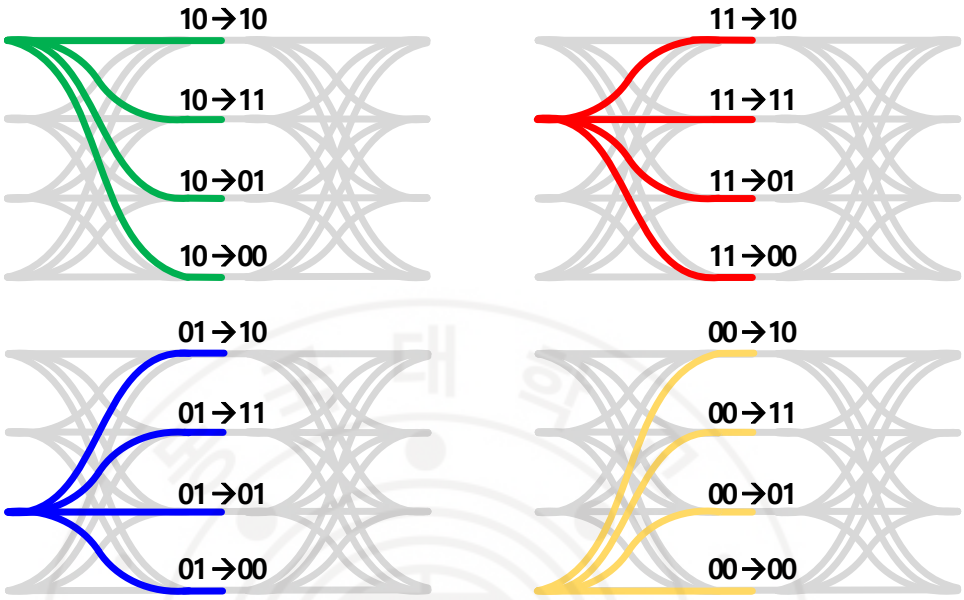


Figure 2.1-4 PAM-4 voltage logic levels

PAM4 modulation, as shown in Figure 2.1-5, allows for doubling the bit rate without doubling the bandwidth in the channel, as compared to NRZ signaling. We have considered the trade-off between SNR and bandwidth. The eye opening of the PAM4 signal is one-third of each NRZ signal, and considering its relationship with SNR, it can be observed that the PAM4 signal is three times more susceptible to noise.

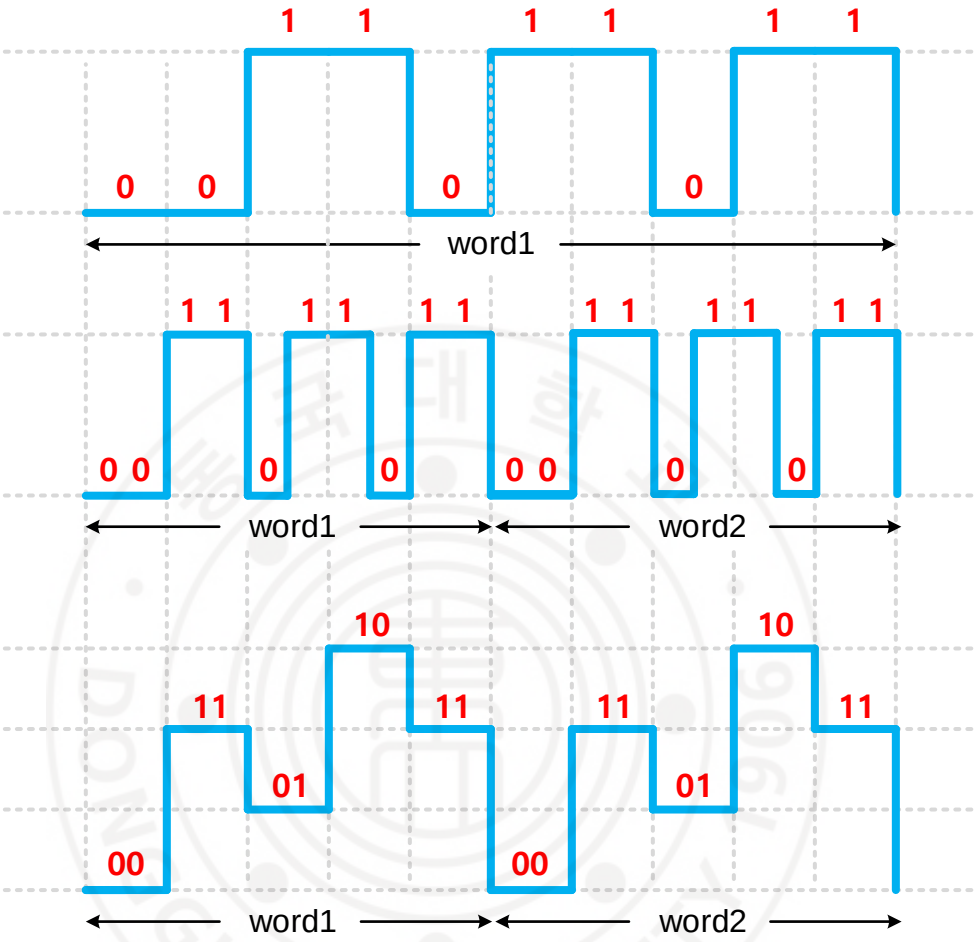


Figure 2.1-5 Comparison between NRZ and PAM-4

2.1.3 Eye diagram

Eye diagram is a common indicator of the quality of signals in high-speed digital transmission systems which provides a simple and useful tool to visualize the interference between data bits. Overlapped voltage waveforms of optical or electrical signals on the time axis within a specific unit time is shown in eye diagram [4].

When the rise and fall times mismatch between the upper and lower eyes, there are possibility of nonlinearity. Linearity of eye diagram can be check with Level Se paration Mismatch Ratio (R_{LM}). This compares the eye heights of the three eyes for med between four levels. If the eye heights of the three eyes are equal or nearly equ al, the value of R_{LM} is nearly equal to 1. The R_{LM} is expressed with equation 2.1-1. The equations required to calculate the R_{LM} are expressed at equation 2.1-2, 2.1-3 and 2.1-4. V_3, V_2, V_1, V_0 is the voltage amplitude of each levels of PAM-4 signal in high order [5].

$$R_{LM} = \text{minimum}((3 \times ES_1), (3 \times ES_2), (2 - 3 \times ES_1), (2 - 3 \times ES_2)) \quad (2.1\text{-}1)$$

$$V_{mid} = \frac{V_0 + V_3}{2} \quad (2.1\text{-}2)$$

$$ES_1 = \frac{V_1 - V_{mid}}{V_0 - V_{mid}} \quad (2.1\text{-}3)$$

$$ES_2 = \frac{V_2 - V_{mid}}{V_3 - V_{mid}} \quad (2.1\text{-}4)$$

Time difference between the centers of each eye is called Eye skew and also one of the indicators that can confirm fidelity [6]. If the center of the three eyes are equal or nearly equal, the value of skew is nearly equal to 0. Eye skew 0/1 – 1/2, 1/2 – 2/3, and 0/1 – 2/3 represents the time difference between the centers of the level 0/1 and level 1/2 eyes, level 1/2 and level 2/3 eyes and level 0/1 and level 2/3 eyes. Figure 2.1-6 shows the eye diagram of ideal PAM-4 signal and represents the 4 level signals, V_{mid} and centers of 3 eye openings.

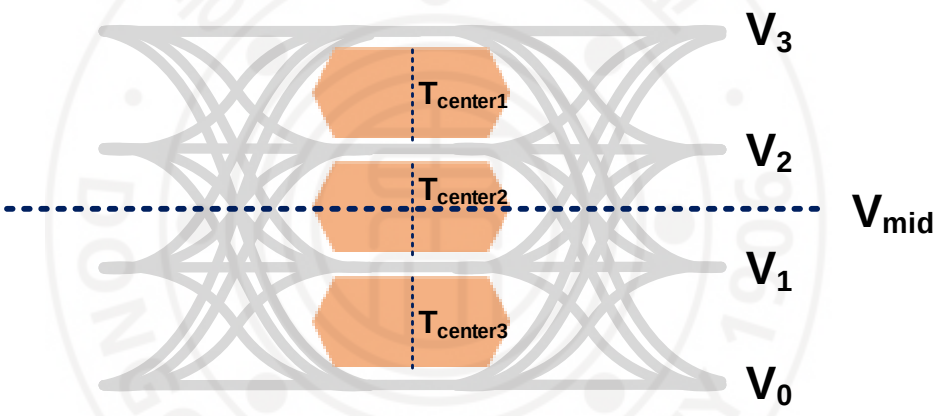


Figure 2.1-6 Eye diagram of ideal PAM-4 signal

2.2 Electro-Optical Modulation Scheme

A signal-controlled electro-optical modulator (EOM) modulates a beam of light using an electro-optical element exhibiting an electro-optic effect. A beam can be modulated by varying its phase, frequency, amplitude, or polarization. EOM scheme can be classified into two categories, External modulation (Indirect modulation) and Direct modulation [7].

2.2.1 External electro-optical modulation (Indirect modulation)

For external electro-optical modulation, modulation is imposed onto the optical signal after the continuous wave is generated. The voltage is modified with the desired signal for the application at the driver before reaching the external modulator [8]. Figure 2.2-1 shows the block diagram of external modulation system.

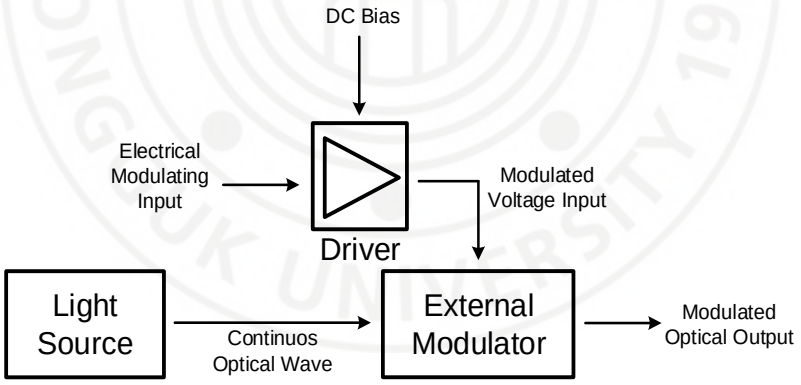


Figure 2.2-1 Block diagram of external modulation system

2.2.2 Direct electro-optical modulation

Direct electro-optical modulation scheme, the current is modified with the desired signal for the application at the driver before reaching the light source. Disadvantage of direct modulation is input current effects electron (charge carrier) density which cause optical output power non-linearity [9]. Figure 2.2-2 shows the block diagram of direct modulation system.

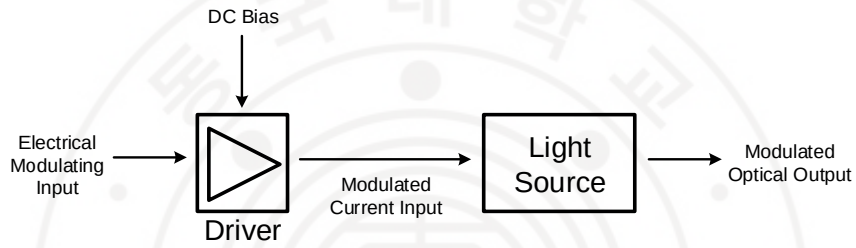


Figure 2.2-2 Block diagram of direct modulation system

2.3 Mach-Zehnder Modulator

The Mach-Zehnder modulator (MZM) is one of the modulators that using an external modulation scheme. MZMs are interferometric structures made from materials with strong electro-optic properties. When electric fields are applied to the MZM electrodes, optical path lengths are changed, resulting in phase modulation. Phase modulation is converted to amplitude (intensity) modulation by combining two arms of different phase modulation [10]. The modulation efficiency of the optical modulator is evaluated at an extended ratio (ER). To get a better Extinction ratio, 180-degree phase shift should be achieved. For the half-wave voltage-interaction length product, $V_\pi \times L$, with longer length of MZM better extinction ratio (ER) can be achieved. The voltage for 180-degree phase modulation is V_π, half-wave voltage, and L is length of the MZM. To achieve 180-degree shift, a driver that amplifies the amplitude of the electrical signal applied to the modulator's electrode. The basic structure of MZM is shown in Figure 2.3-1. With the electrical signals V+ and V-, the optical input is split into upper and lower modulator arms, which are phase modulated with phase shifters. The amplified electrical modulating signal from the driver is injected to blue electrode and signal’s voltage makes the EOM is occurred.

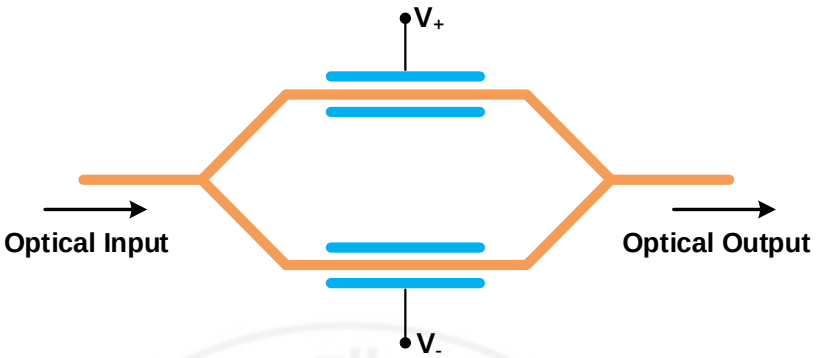


Figure 2.3-1 Basic structure of MZM

MZM can be classified into two categories, traveling wave MZM and segmented electrode MZM.

2.3.1 Traveling wave MZM

The traveling wave MZM is most widely employed in commercial MZMs. It has good thermal insensitivity, high robustness to process and temperature variation. Also, it expands the effective electrical bandwidth by absorbing the electrode's capacitive loading. During electro-optical modulation, the electrical and optical propagation velocities naturally match without additional design. With many advantages, but there is also drawback of modulation efficiency. High level of driving swing is essential because of high resistivity of the on-chip metal wires make the transmission line lossy, which attenuate the driving swing [11]. The architecture of traveling wave MZM is shown in Figure 2.3-2.

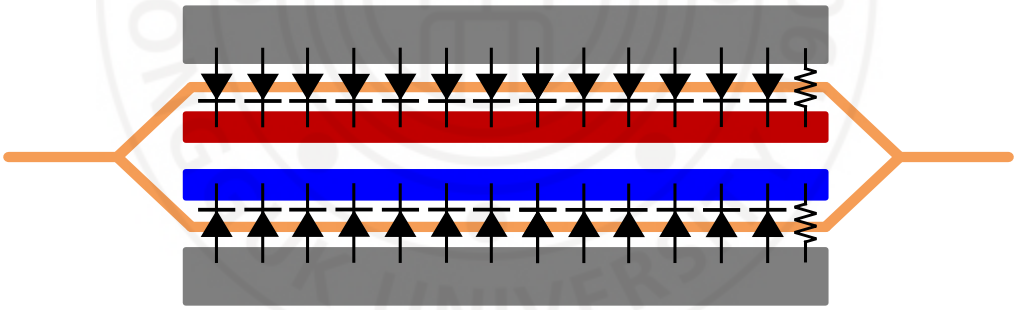


Figure 2.3-2 Architecture of Traveling wave MZM

2.3.2 Segmented electrode MZM

The segmented electrode MZM is a separated form of traveling wave MZM. So, the modulator can be a lumped capacitor which consumes much less power than a transmission line. It is possible to use drivers with smaller output swings, resulting in smaller chip areas. To drive each separated MZMs, same amount of drivers with electrodes are required. An additional phase shifter must be designed for every segmented parts in order to match the propagation velocity of electrical and optical signals [12]. Due to complicated integration from the structure, multiple connections are required. The architecture of segmented electrode MZM is shown in Figure 2.3-3.

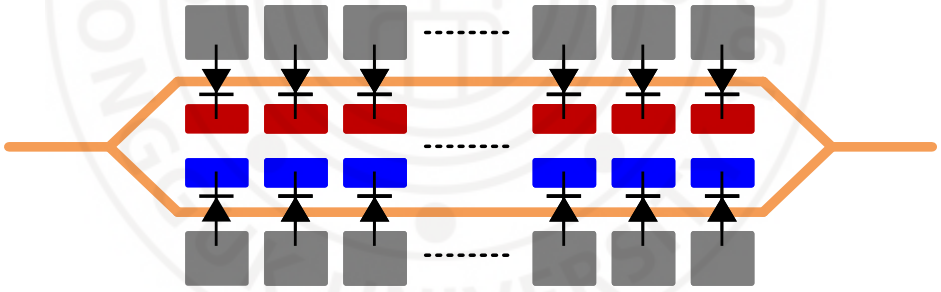


Figure 2.3-3 Architecture of Segmented electrode MZM

Chapter 3 Ultra-Wideband MZM Driver

In a pulse-based communication system, the range resolution is inversely proportional to the pulse width [13]. High data rate transfer system like 200Gb/s silicon photonics optical transmitters, it is vital to design and manufacture integrated high-speed driver ICs [14]. To make Driver must be able to provide wide bandwidth over 50 GHz and output voltage swing when connected to a silicon photonics based MZM. Meanwhile, the fidelity is guaranteed which means the eye openings of output signal's eye diagram is well defined. Figure 3.1-1 shows the architecture of proposed EOM system. In this work, two distributed amplifiers (DA) are designed on a single chip for driving two separated electrodes of a traveling wave MZM. The traveling wave MZM is separated for the advantage of modulation efficiency with reduced resistivity of the on-chip metal wires [10 -11]. In that regard, proposed driver is designed single differential input enables dual driving of DA 1 and DA 2 with Wilkinson divider and microstrip based delay line.

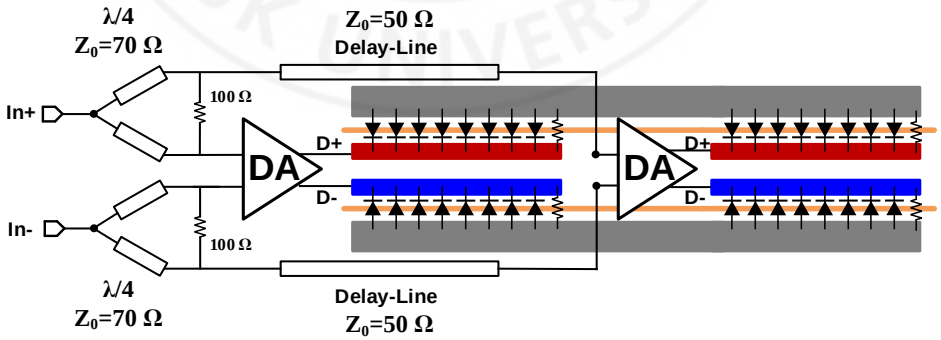


Figure 2.3-1 Architecture of the proposed EOM system

3.1 Distributed Amplifier Design

General amplifiers are tuned and matched using the capacitance component of transistors, which limits the amplifier's bandwidth since the wideband characteristics of input and output matching networks cannot be achieved. With distributed amplifiers, transistors' parasitic capacitance is absorbed by the transmission line's inductance, resulting in flat gain and wideband characteristics of input and output matching networks. Even if the parasitic capacitance component changes due to the inaccuracy of the transistor model, the change in circuit characteristics is less sensitive than other amplifiers [15].

3.1.1 Structure of distributed amplifier

A distributed amplifier consists of cascaded unit cells. Equation 3.1-1 expresses the voltage gain of DA. N represents the number of distributed stages, and G_m' represents the transconductance of a single unit cell. DA1 is utilized with seven stages to transmit the high swing PAM-4 signals to MZM electrodes.

$$G_v = N\frac{G_m' Z_0}{2} \tag{3.1-1}$$

A distributed amplifier's input equivalent inductance is L_{in}, its input equivalent capacitance is C_{in}, its output equivalent inductance is L_{out}, and its output equivalent capacitance is C_{out}. Equation 3.1-2 describes the input characteristic

impedance Zin, while equation 3.1-3 describes the output characteristic impedance Zout.

$$Z_{in} = \sqrt{\frac{L_{in}}{C_{in}}} \tag{3.1-2}$$

$$Z_{out} = \sqrt{\frac{L_{out}}{C_{out}}} \tag{3.1-3}$$

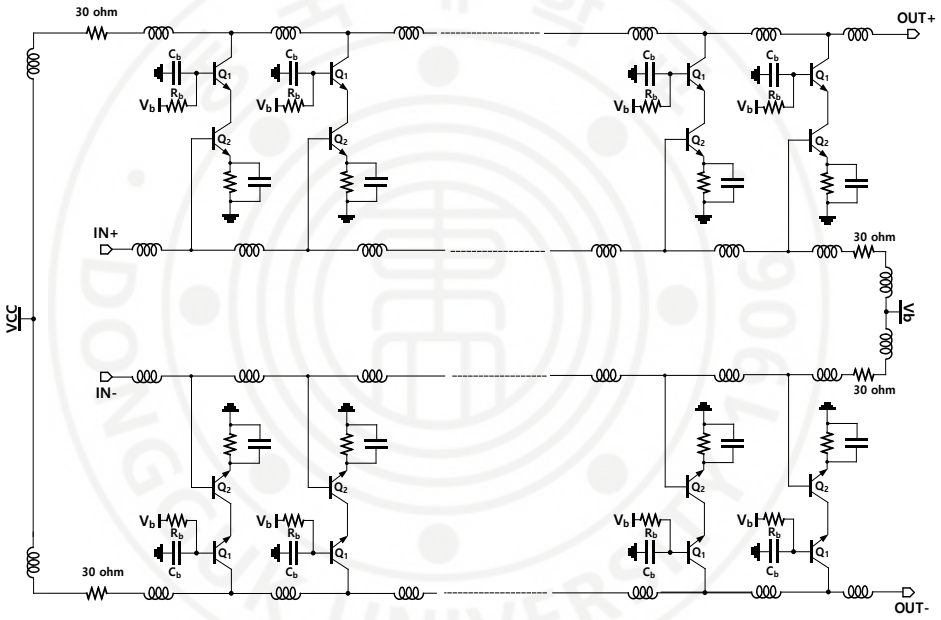


Figure 3.1-1 Schematic of differential distributed amplifier

Figure 3.1-2 shows the schematic of differential distributed amplifier. In order to absorb the reflected signal maximally, the termination resistor is used in the opposite direction of the input and output terminals. Ideally, termination resistor value must be matched with Z_{in} and Z_{out} which are 50 Ohm. But, in this work the

collector bias is applied through the termination resistor so considering the efficiency, 30 Ohm resistor is used. The reflection coefficient Γ is calculated by equation 3.1-4 and the return loss (RL) is calculated by equation 3.1-5. Even the termination resistor is 30 Ohm, the RL is 12dB which is an affordable value.

$$\Gamma = \frac{Z_L - Z_o}{Z_L + Z_o} \tag{3.1-4}$$

$$\mathrm{RL} = -20\log_{10}|\Gamma|^2 \tag{3.1-5}$$

As mentioned, distributed amplifier achieves impedance matching with transistor's parasitic capacitance is absorbed by the transmission line's inductance which called artificial transmission line. Figure 3.1-3 shows the artificial transmission line equivalent circuit. The artificial transmission line is formed with BJT's input/output capacitance and microstrip based transmission line's inductance in this work.

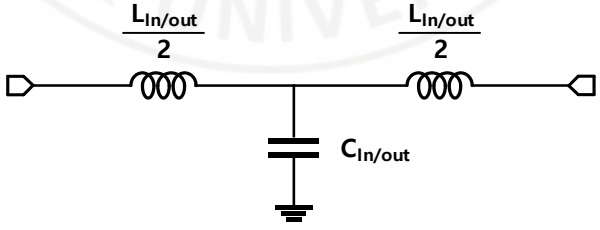


Figure 3.1-2 Artificial transmission line equivalent circuit

3.1.2 Unit cell design

To achieve 200Gb/s PAM4 signal transfer with DAs, it is essential to interpret the dominant bandwidth limiting factors form parasitic components. The operation of a DA is based on the parasitic capacitance of transistors are absorbed into base and collector T-lines to form two wideband low-pass filter-like structure in which each unit cells are embedded.

There is series loss and shunt loss at T-line. The series loss is caused by the metal resistance which is proportional to the length of the T-line and determined by the input capacitance of the unit cell. The shunt loss is caused by the resistive loading from the unit cell which is proportional to the input conductance. In order to minimize input capacitance as well as input conductance, it is important to minimize both of them.

Due to the base resistance of bipolar transistors, there is relatively large effective input capacitance and conductance. Because of skin depth at high frequency, Series resistance tends to increase with frequency because T-line series resistance is proportional to square root of frequency. High frequency shunt losses result from an increase in input conductance, limiting bandwidth at higher frequencies. By using cascode unit cells, the collector capacitance is much lower than the base capacitance, and the output conductance can also be reduced significantly. In that regard, at this thesis the analysis is focused on baseline. The large high-frequency baseline loss reduces bandwidth and power contribution from final unit cell stages near the load,

defeating the purpose of amplification. The resistive emitter degeneration can be used to mitigate the baseline loss.

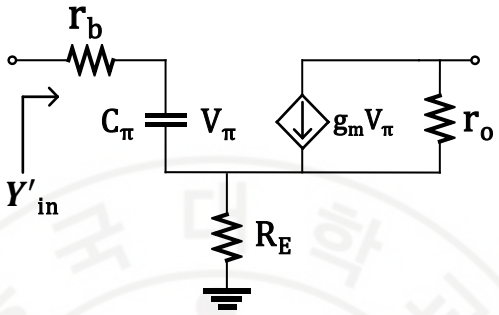


Figure 3.1-3 High-frequency small-signal equivalent of standard common emitter

By using a high-frequency small-signal equivalent circuit of standard common emitter, as shown in Figure 3.1-5, input capacitance and input conductance are given by equation 3.1-6 and 3.1-7, respectively.

$$C_{in} = \frac{C_\pi}{1 + w^2 {C_\pi}^2 {r_b}^2} \tag{3.1-6}$$

$$G_{in} = \frac{w^2 {C_\pi}^2 r_b}{1 + w^2 {C_\pi}^2 {r_b}^2} \tag{3.1-7}$$

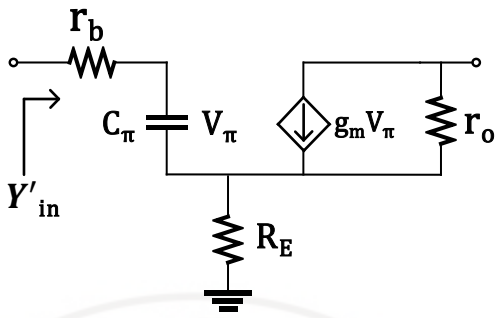


Figure 3.1-4 High-frequency small-signal equivalent of degenerated common emitter

Figure 3.1-6 illustrates high-frequency small-signal equivalent circuit of degenerated common emitter in which the input capacitance and input conductance can be calculated using equation 3.1-8 and 3.1-9, respectively.

$$C'_{in} = \frac{\frac{C_\pi}{1+g_m R_E}}{1+w^2\left(\frac{C_\pi}{1+g_m R_E}\right)^2+(r_b+R_E)^2} \tag{3.1-8}$$

$$G'_{in} = \frac{w^2\left(\frac{C_\pi}{1+g_m R_E}\right)^2+(r_b+R_E)}{1+w^2\left(\frac{C_\pi}{1+g_m R_E}\right)^2+(r_b+R_E)^2} \tag{3.1-9}$$

It is possible to effectively reduce both the input capacitance and the input conductance by increasing the degeneration resistor. Also, the effective transconductance of the transistor is reduced, and it can be expressed as equation

3.1-10 with a 3-dB bandwidth of equation 3.1-11.

$$G_m = \frac{g_m}{(1 + g_m R_E)\left(1 + j\frac{w}{w_{p,gm}}\right)} \quad (3.1\text{-}10)$$

$$w_{p,gm} = \frac{1 + g_m R_E}{(r_b + R_E)C_\pi} \quad (3.1\text{-}9)$$

It is possible to create a high-frequency zero at $w_z = \frac{1}{R_E C_E}$ by adding a degeneration capacitor in parallel to the degeneration resistor which can enhance the bandwidth. As a result, the peaking caused by the zero partially cancels the roll-off caused by the dominant pole and extends the bandwidth. The new transconductance is given by equation 3.1-12. Through the new transconductance equation, it is checked that the transconductance of the unit cell is scaled down by R_E and C_E.

$$G'_m = \frac{g_m(1 + jwR_E C_E)}{(1 + jwr_b C_\pi)(1 + jwR_E C_E) + (g_m + jwC_\pi)R_E} \quad (3.1\text{-}12)$$

In order to preserve resistive degeneration for in-band frequencies, the zero should be higher than $w_{p,gm}$. Degeneration resistor and degeneration capacitor values are evaluated in order to obtain an optimal small-signal design point. The DA bandwidth can be significantly enhanced along with the gain bandwidth (GBW) product by increasing the degeneration resistance. This is primarily due to the reduction in loaded baseline loss at high frequency. However, increasing degeneration resistance further reduces loaded baseline loss, but also degrades GBW

core transistors [16]. So, the value of effective resistance and capacitance of unit cell was carefully decided in this work. With this analysis, unit cell topology has determined to use RC degenerated with advantage of wide bandwidth, low loss.

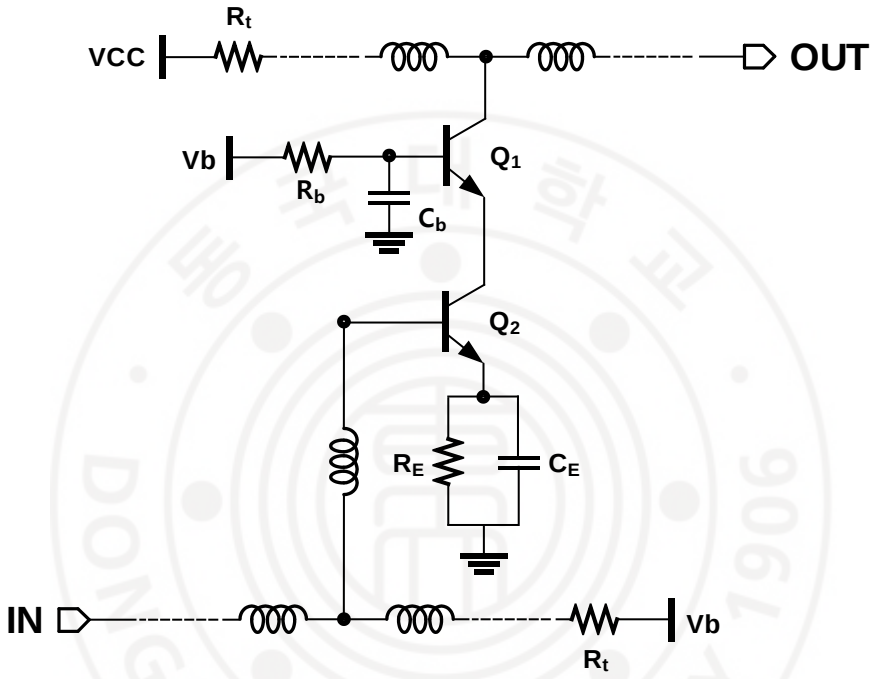


Figure 3.1-5 Schematic of unit cell

Figure 3.1-4 shows schematic of unit cell. Unit cell is designed with a degenerated cascode structure in which the common emitter amplifier's collector and common base amplifier's emitter are combined. With this topology unit cell can have higher gain than the standard degenerated structure. The size of the transistors, capacitor and resistor values are listed in Table 3.1-1. Due to low collector capacitance, the cascode bipolar transistor Q1 is sized larger than the Q2. For the input base

transmission line and output collector transmission line inductance value is estimated 28pH and 23pH respectively which makes the input and output characteristic impedance as single ended 50 Ohm.

Table 3.1-1 List of the components value in the proposed Driver's DA unit cell

Component	**Value**	**Component**	**Value**
Q_1	10*70 nm/ 900nm	C_b	120 fF
Q_2	6*70 nm/ 900nm	R_b	2 kOhm
R_t	30 Ohm		

3.2 Tuning Network Design

In this work, for the purpose of the control the gain of in-band and out-of-band as well as the eye opening of eye diagram the tunable RC network is implemented at degeneration. In initial design level, by changing the resistance and capacitance of lumped resistor and capacitor simulated S-parameter simulation.

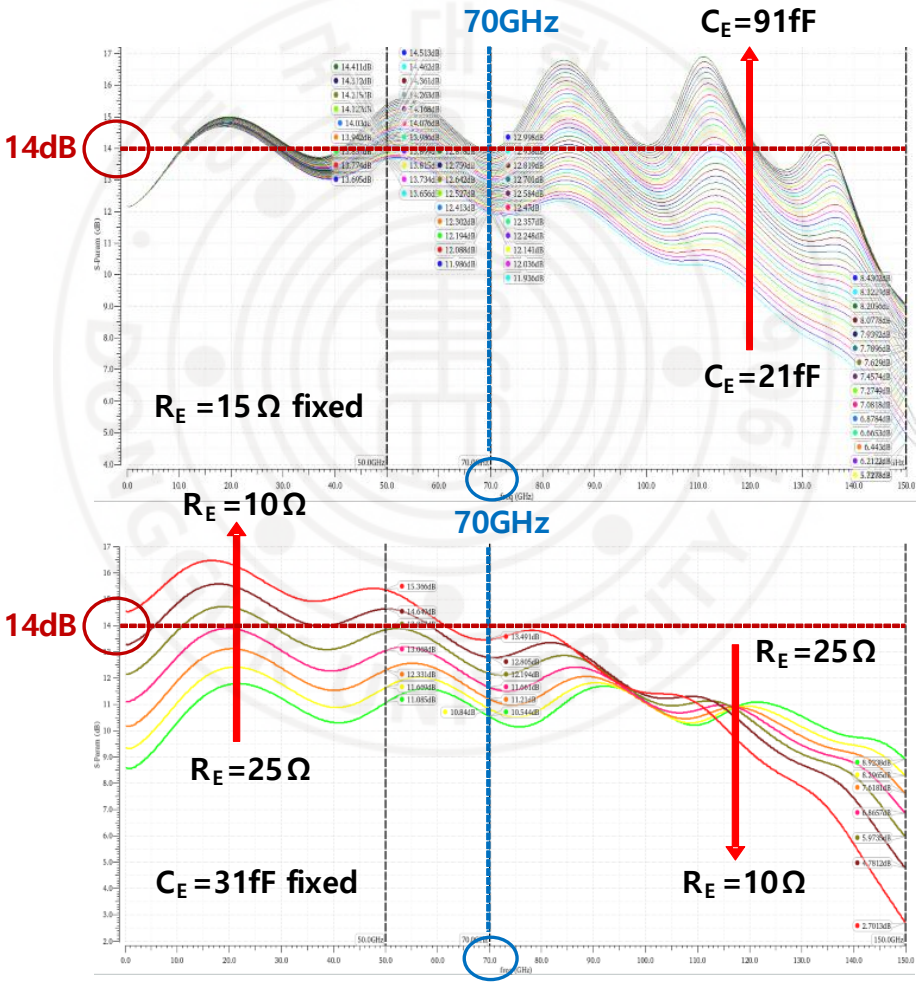


Figure 3.2-1 S-parameter (S21) with sweep R, C values

Figure 3.2-1 shows S-parameter (S21) with sweep R, C values. The bigger the degeneration capacitor value, the bandwidth became more wider because of the high frequency Zero peaking the high frequency gain. In reverse, the smaller the degeneration capacitor value, the better the eye opening of the eye diagram with lower gain at high frequencies. For the resistor, as the resistance value decreased, the bandwidth decreased and the low frequency gain increased while the high frequency gain decreased because of baseline loss get bigger. The eye opening improved as the resistance values decreased, and after 30Ω or less, the eye opening deteriorated. In order to these effects, the resistance and capacitor tuning system is designed as a bank (RC bank) with its value determined by the MOSFET switch. The effective resistance and capacitor values of the degeneration resistor and capacitor are changed by on/off sate of switch. The tuning range was determined by balancing the trade-off between bandwidth, gain, and eye opening depending on the effective capacitance and resistance values.

3.2.1 SPI-Scanchain

Each switch for RC bank is controlled by output control bit of SPI Scan-chain, a Serial-input / Parallel-output interface. A 32-bit SPI Scan-chain is implemented with four 8-bit cells connected parallel, 32-bit cells, and a scan-chain that allows MOSI signal input by selecting a cell from the four chains to which the clock is input. Cell selector, non-overlapping clock generator, a circuit that prevents errors from occurring because the rising and falling edges of the clock overlap, inputs MOSI input containing bit information to the circuit during the first communication, and outputs MISO during the second communication. In order to ensure that bit information is smoothly communicated to the circuit, a MOSI/MISO selector is included. On/off control of the RC Bank switch can be achieved using the 32 SDATA outputs of the Scan-chain. Figures 3.2-2, 3.2-3 and 3.2-4 show the block diagram, layout, and simulation result of 32bit SPI Scan-chain respectively. It is confirmed that the serial MOSI signal is output in parallel when the first 8 bits and the last 8 bits are input to 101010.

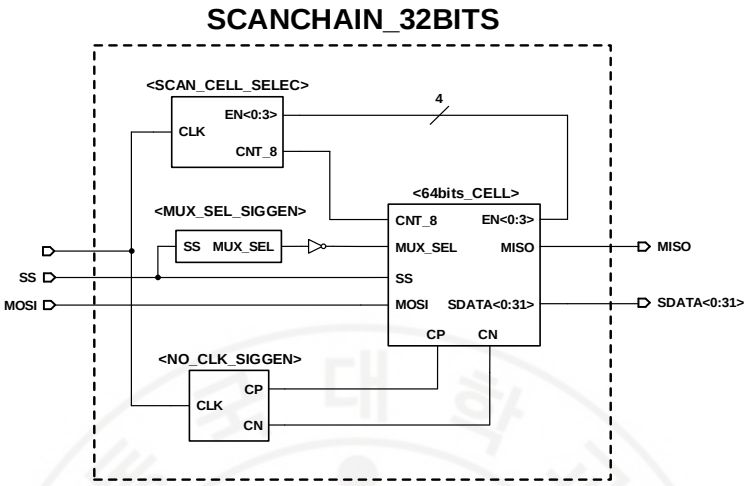


Figure 3.2-2 Block diagram of 32bit SPI Scan-chain

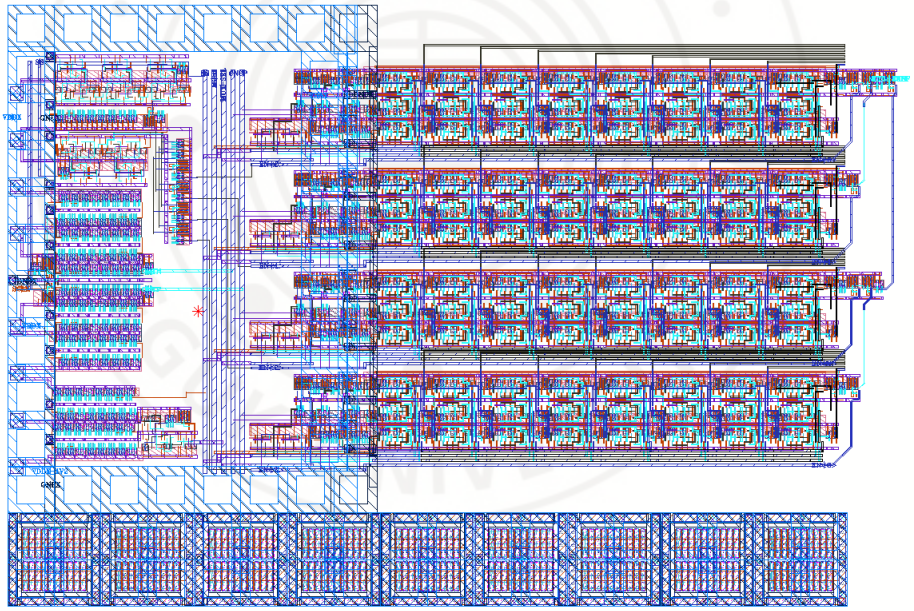


Figure 3.2-3 Layout of 32bit SPI Scan-chain

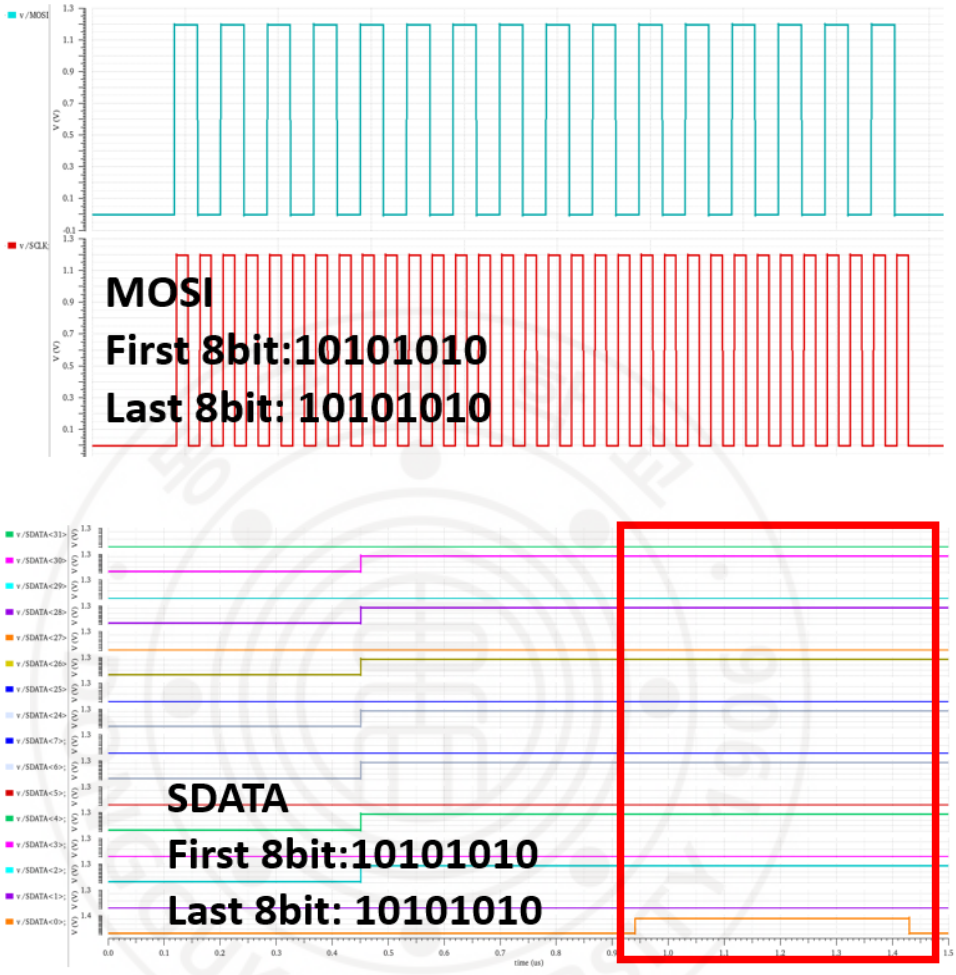


Figure 3.2-4 Simulation result of 32bit SPI Scan-chain

3.2.2 Capacitor bank design

The capacitor bank (C bank) is designed with capacitors connected in series with MOSFET switch and these pairs are connected in parallel. Then the number of switches turned on is increased, the effective capacitance become higher. 16 switches are used in the C bank considering the tuning range. To control the 16 switches, a 4to15 binary to thermometer decoder's output bit and one control bit from Scanchain was used. The 4 scan-chain output bits control the 15 switches of the capacitor bank. This can be achieved by using decoder. The schematic and layout of the designed 4to15 binary to thermometer decoder for C bank control are shown in Figure 3.2-5 and 3.2-6, respectively.

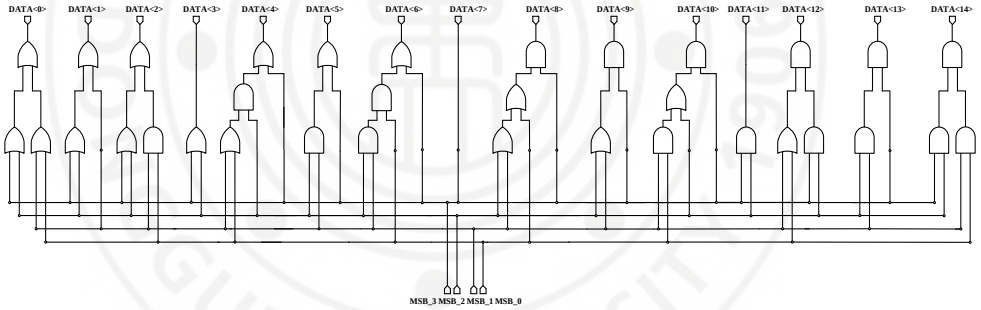


Figure 3.2-5 Schematic of 4to15 binary to thermometer decoder

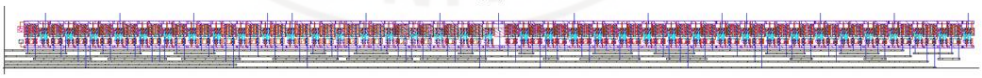


Figure 3.2-6 Layout of 4to15 binary to thermometer decoder

According to decoder input bits, Table 3.2-1 summarizes the number of turn on switches with each decoder input bit.

Table 3.2-1 Number of turn on switches with each decoder input bit

Decoder Input (MSB1/2/3/4)	**Switch On** (Cap added)	**Decoder Input** (MSB1/2/3/4)	**Switch On** (Cap added)
0000	0	1000	8
0001	1	1001	9
0010	2	1010	10
0011	3	1011	11
0100	4	1100	12
0101	5	1101	13
0110	6	1110	14
0111	7	1111	15

The schematic, layout and simulated effective capacitance of designed C bank are shown in Figure 3.2-7, 3.2-8 and 3.2-9, respectively. The capacitor C_1 value is 3.6 fF and transistor M_1 value is 36.3um(W)/130nm(L). And the tuning range of effective capacitance is 46.8 fF to 64.1 fF with around 1.2 fF interval at 70GHz.

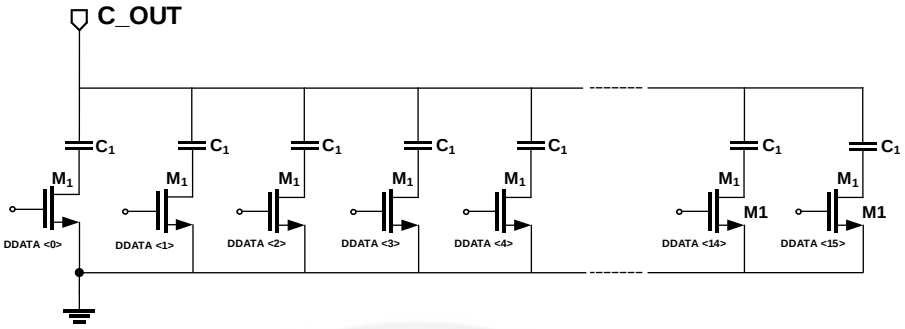


Figure 3.2-7 Schematic of designed C Bank

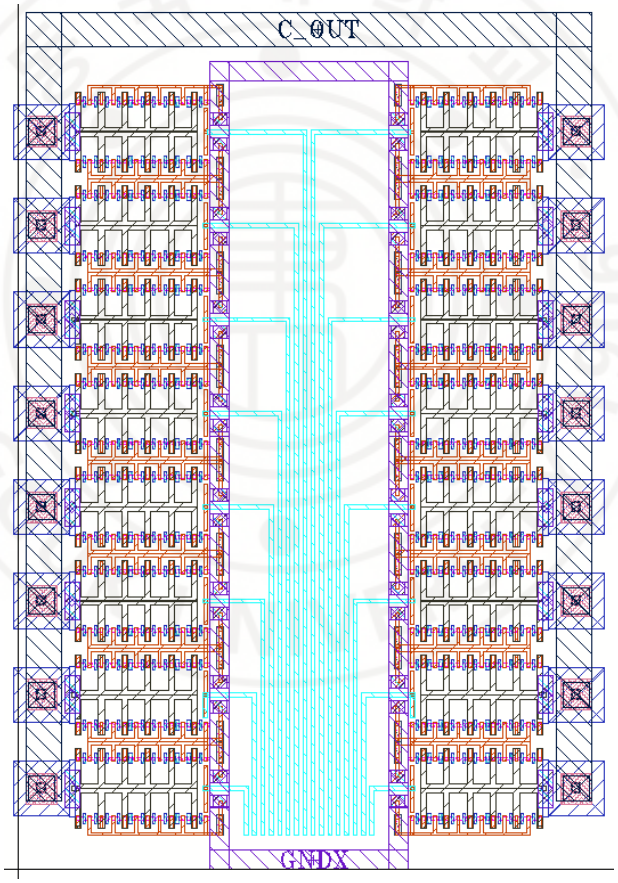


Figure 3.2-8 Layout of designed C Bank

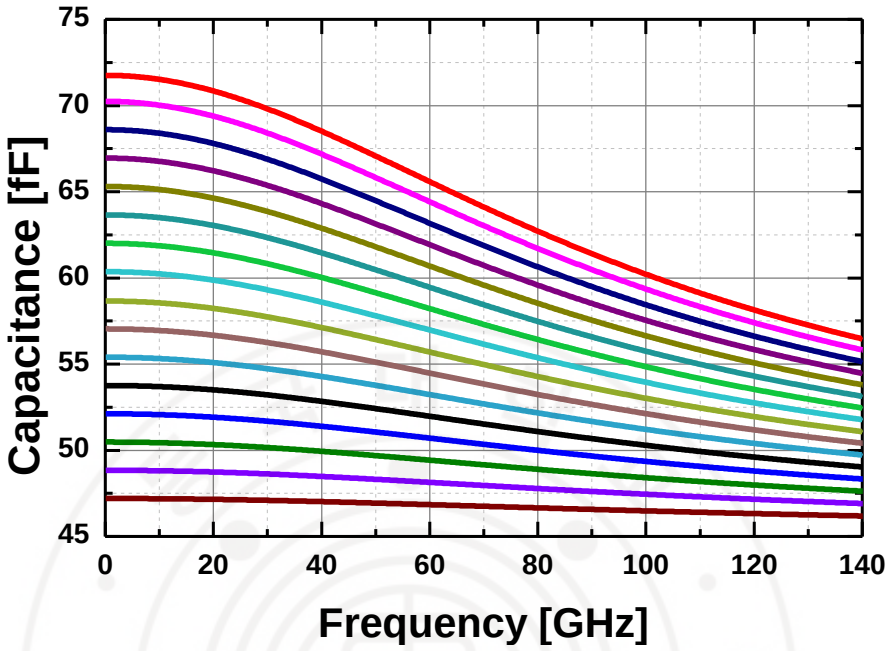


Figure 3.2-9 Simulated effective capacitance of designed C Bank

3.2.3 Resistor bank design

Based on the characteristic that the channel resistance changes according to the gate voltage of the MOSFET, we implemented the resistor bank (R bank) as a parallel structure of a variable resistor (MOSFET channel) and a fixed resistor. The MOSFET's channel resistance is controlled by gate bias voltage. In this work, voltage divider that distributing a voltage between a series-connected switch and a parallel-connected resistor structure is used for gate bias voltage. One fixed resistor is connected to five parallel pairs of series-connected switch and resistor, with the input voltage applied across the fixed resistor and the output voltage emerging from

the connection between them. Each resistance value of the five parallel pairs has a double difference in the range from 3 kOhm to 48 kOhm. When the switch is switched on, the resistance become effective. The combination of parallel resistance can control the channel resistance. The schematics of R bank control voltage divider and R bank are shown in Figure 3.2-10. Table 3.2-2 summarizes list of the components value in the R bank control voltage divider and R bank.

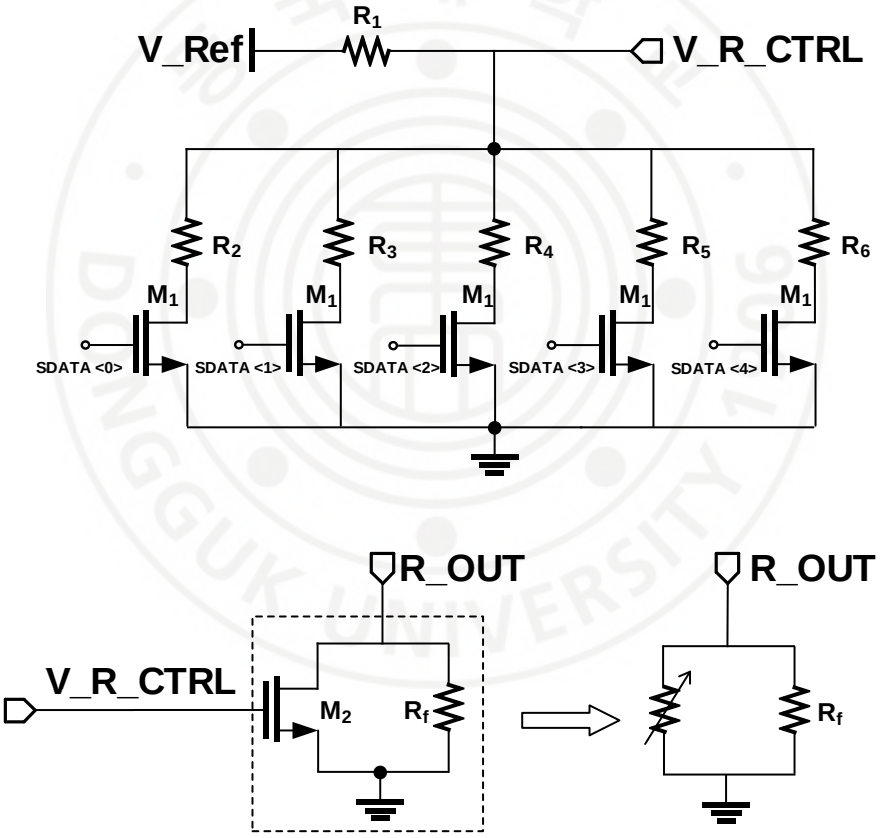


Figure 3.2-10 Schematics of R bank control voltage divider and R bank

Table 3.2-2 List of the components value in the R bank control voltage divider and R bank

Component	Value	Component	Value
R_1	12 kOhm	R_6	3 kOhm
R_2	48 kOhm	R_f	10 Ohm
R_3	24 kOhm	M_1	18.15um/130nm
R_4	12 kOhm	M_2	39.48um/450nm
R_5	6 kOhm		

The Layout of designed R bank control voltage divider and R bank are shown in Figure 3.2-11. To generate the R bank control voltage, two resistors in series with a switch are connected in parallel with a resistor in parallel with the resistor in series with the switch.

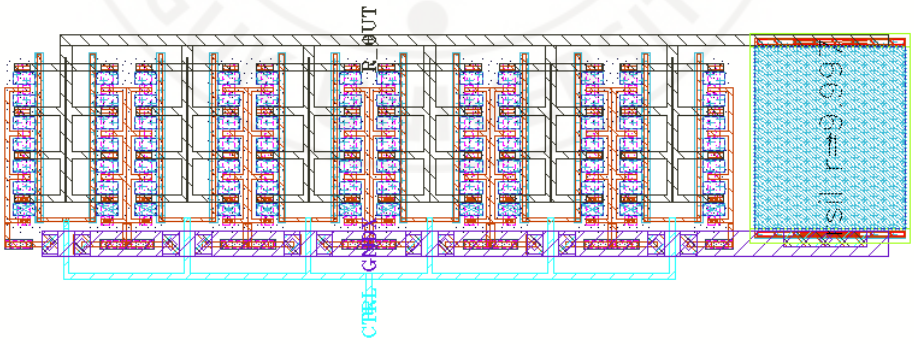


Figure 3.2-11 Layout of designed R bank control voltage divider and R bank

Figure 3.2-12 shows the voltage range of R bank control voltage divider and figure 3.2-13 shows the effective resistance of R bank. Designed R Bank control voltage divider can control 0.3V to 2.5V range. When R bank control voltage is 2.5V and 0.3V, effective resistance of R bank is 13.4 Ohm and 17.3 Ohm respectively.

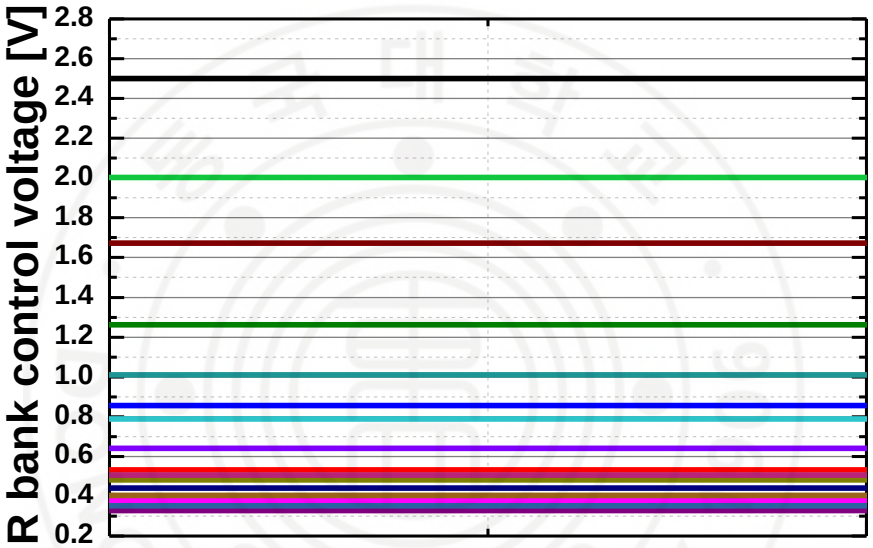


Figure 3.2-12 Simulated Voltage range of R bank control voltage divider

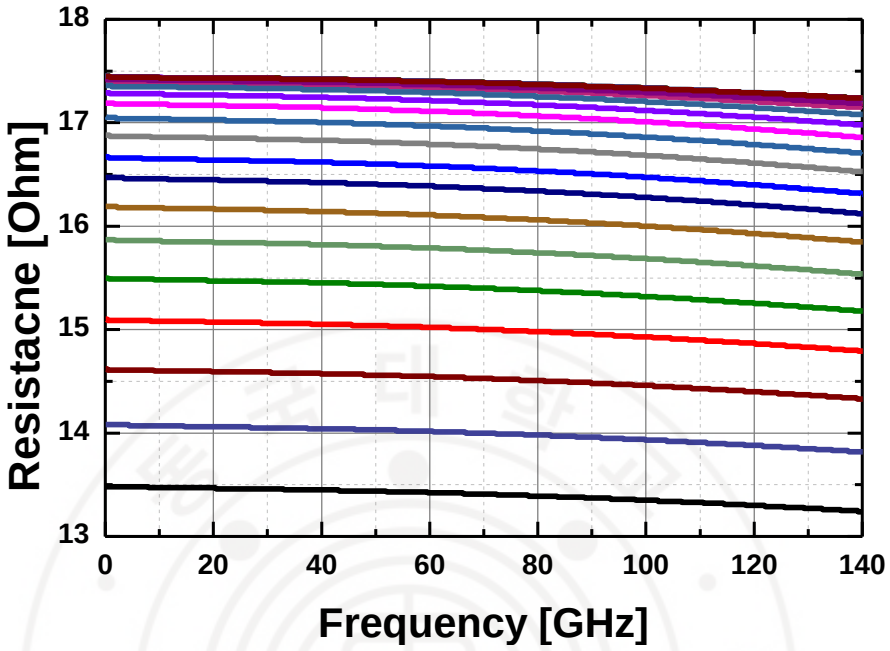


Figure 3.2-13 Simulated Effective resistance of R bank

3.3 Standalone Distributed Amplifier Simulation Results

C bank and R bank are used at degeneration of each unit cell in this thesis. Therefore, all the simulation's capacitor bank control bit state and resistor bank control voltage are presented with figures. For the C bank, the on/off state of the switch with five digits, the first four numbers for 4to15 binary to thermometer decoder which are control 15 switches, and the last one for switch that is not controlled by decoder. The R bank control voltage indicates the node voltage generated by the on/off state of the voltage divider switches. The collector bias for the standalone DA1 was 6.3V. For the base bias of the common emitter amplifier part (Q2) was 1.1V and common base amplifier part (Q1) was 2.5V.

3.3.1 Simulation results

The simulated S-parameters of the designed standalone 7stage DA under C bank ctrl bit : 11111 / R bank ctrl voltage 1.3 V condition are shown in Figure 3.3-1. The standalone 7stage DA achieves a 3-dB gain bandwidth of 110 GHz (10 kHz–110 GHz) a peak gain of 14.9 dB. Within the 3-dB gain bandwidth, input and output return losses are greater than 5 dB. Also, Figure 3.3-2 shows simulated results of the large-signal performance under C bank ctrl bit : 11111 / R bank ctrl voltage 1.3 V condition. The simulated saturated output power and the 1-dB compressed output power (OP1dB) are 18.2 dBm and 16.6 dBm at 70 GHz, respectively. For the peak power added efficiency (PAE) is around 5% because of power dissipation from termination resistor at collector bias line as mentioned at Chapter 3.1.1.

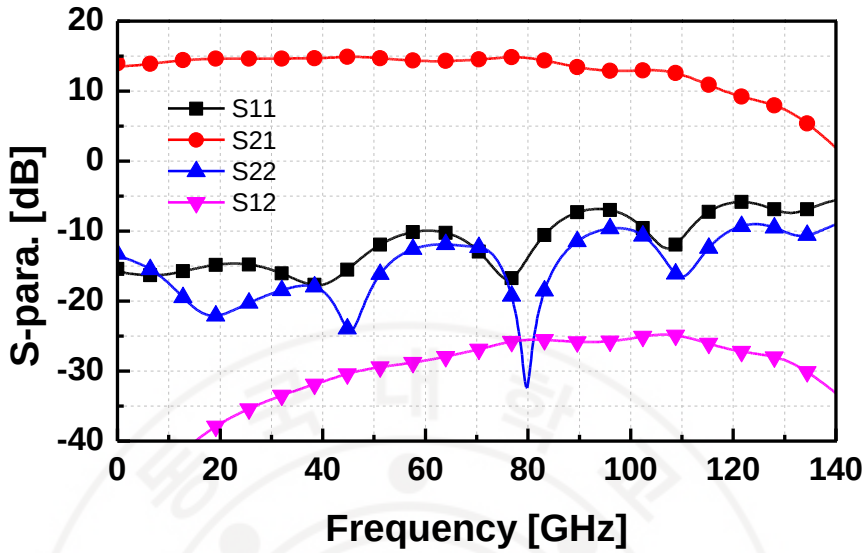


Figure 3.3-1 S-parameter simulation results of 7stage DA
under C bank ctrl bit : 11111 / R bank ctrl voltage 1.3 V condition

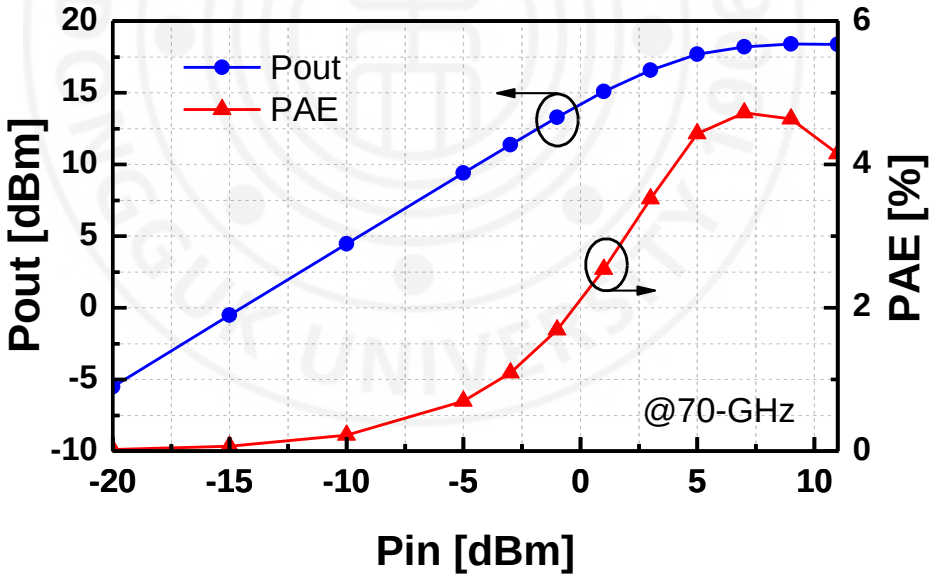


Figure 3.3-2 Large signal simulation results of 7stage DA at 70 GHz
under C bank ctrl bit : 11111 / R bank ctrl voltage 1.3 V condition

3.3.2 Eye diagram simulation result

The Eye diagram simulation result of 7stage DA under C bank ctrl bit : 11111 / R bank ctrl voltage 1.3 V condition is shown in Figure 3.3-3 based on transient simulation of 7stage DA with 1Vppd 200Gb/s PAM-4 input signal. We can check the 3 eye openings are clear with over 5Vppd output swing during 1Vppd input and Eye linearity and skew are 1 and 0, respectively.

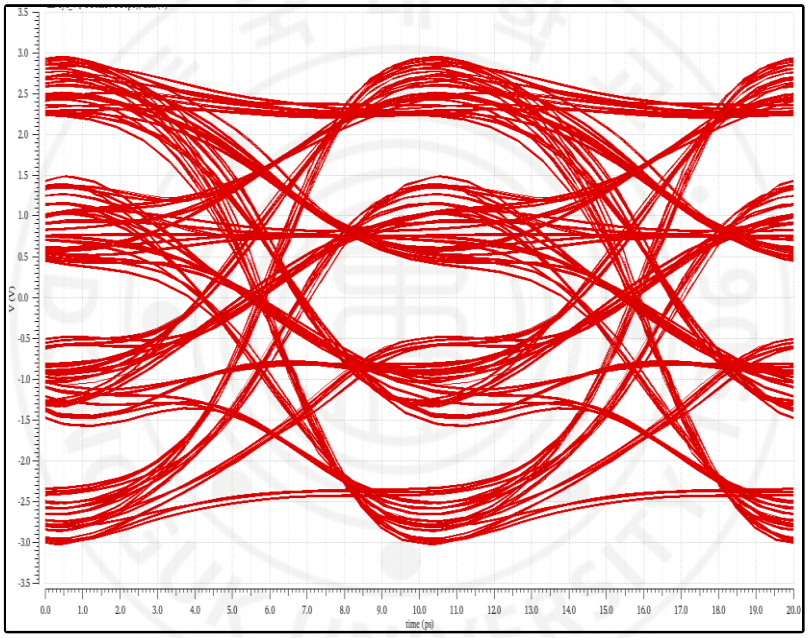


Figure 3.3-3 Eye diagram simulation result of 7stage DA under C bank ctrl bit : 11111 / R bank ctrl voltage 1.3 V condition

3.4 Synchronization

In order to check synchronize the optical signal and electrical signal, it is necessary to check the signals separated by Wilkinson power divider. Also, the transition between MZM and driver has considered. Figure 3.4-1 shows the architecture of the proposed EOM system with transition.

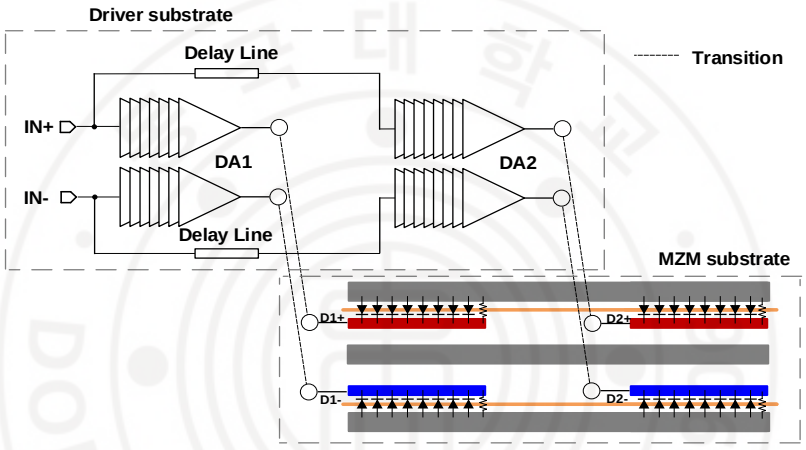


Figure 3.4-1 Architecture of the proposed EOM system with transition

The following path will be taken in this work in order to determine whether the optical and electrical propagations coincide with the input signal divided through the Wilkinson divider and passed through DA, optical waveguide and MZM structure.

Path 1: DA1(τ_{DA1}) → Transition between MZM pads and DA pads1(τ_{PAD1}) → MZM1(τ_{opt_MZM1}) → Optical waveguide(τ_{opt_delay})

Path 2: MSTL delay line(τ_{delay_line}) → DA2(τ_{DA2}) → Transition between MZM pads and DA pads2(τ_{PAD2})

Verify that synchronize of the electrical and optical signals that have passed

through the two paths are identical at the point where the eye opening of the eye diagram is maximized on the time domain. Figure 3.4-2 shows the block diagram for delay analysis. To meet the synchronization of proposed system, delay time of each components should satisfy equation 3.3-1.

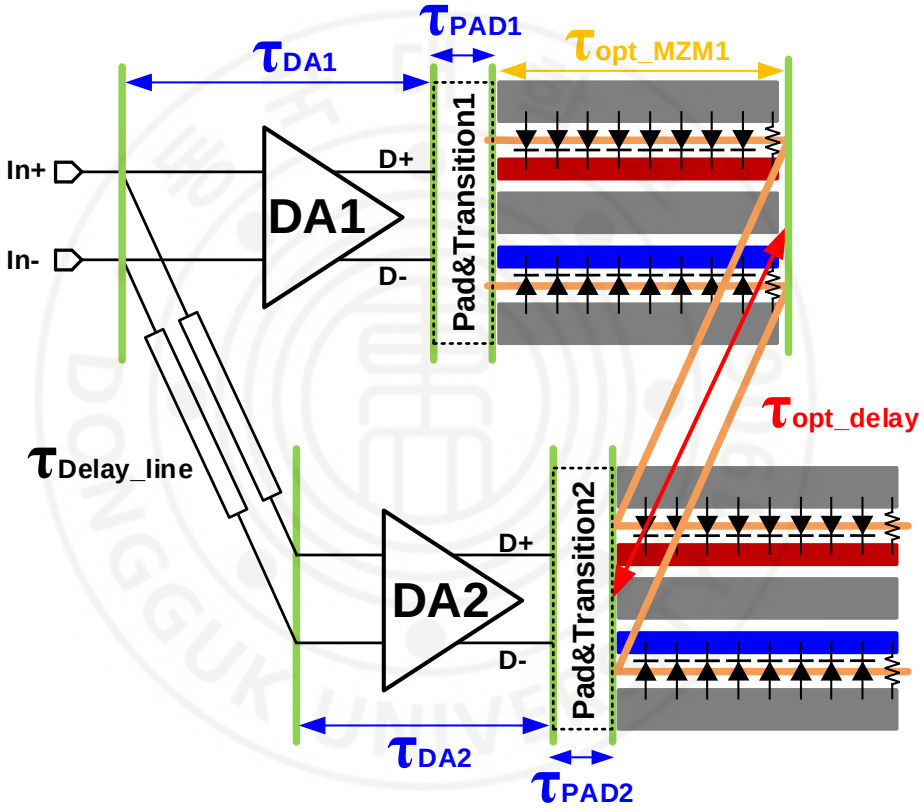


Figure 3.4-2 Block diagram for delay analysis

$$\tau_{DA1} + \tau_{PAD1} + \tau_{opt\_MZM1} + \tau_{opt\_delay} = \tau_{delay\_line} + \tau_{DA2} + \tau_{PAD2} \quad (3.3\text{-}1)$$

Using the lossless ideal transmission line model of cadence virtuoso, a design tool, the time delay of MZM (924um) and optical waveguide (1545um) were compensated during the transient simulation. Delay time of optical waveguide can be calculated by equation 3.3-2.

$$Delay\ time\ = \frac{n}{c} \times\ waveguide\ length \tag{3.3-2}$$

n is effective refractive index and c is velocity of light in vacuum. The effective refractive index of MZM and optical waveguide is 3.96 and 4.36 respectively. With the effective refractive index, delay time of the ideal transmission line models were determined 12.2 psec for the MZM (924um) and 22.5 psec for the optical waveguide (1545um), which have total delay of 34.7 psec.

3.4.1 Wilkinson divider design

In a dual driving design with two driving amplifiers with one input and one output, a Wilkinson divider was used to distribute the input signal between the two driving amplifiers. The Wilkinson divider matches each of the three ports with 50 Ohm while maintaining a high isolation [17], so the signals reflected from DA1 and DA2 are absorbed in the resistance between the output ports and do not interact. Figure 3.4-3 and 3.4-4 show the layout of designed Wilkinson divider and 3D-EM model of designed Wilkinson divider based on HFSS. For the compact design at limited chip area, $\lambda/4$ transmission line is meandered. The simulated S-parameters of the designed Wilkinson divider are shown in Figure 3.4-3. There is a 3.6dB insertion loss at 50GHz and a 3.6dB insertion loss at 70GHz due to Wilkinson divider.

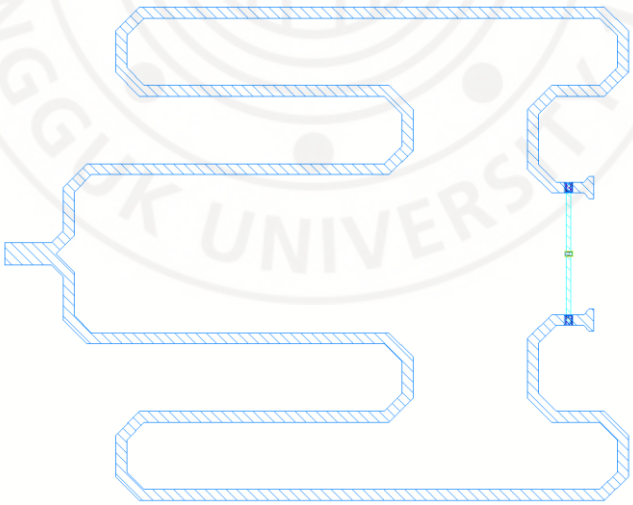


Figure 3.4-3 Layout of designed Wilkinson divider

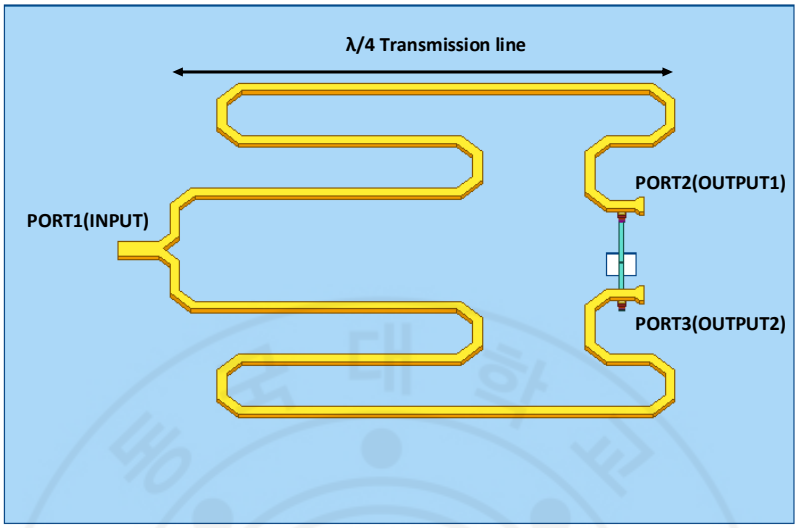


Figure 3.4-4 3D-EM model of Wilkinson divider based on HFSS

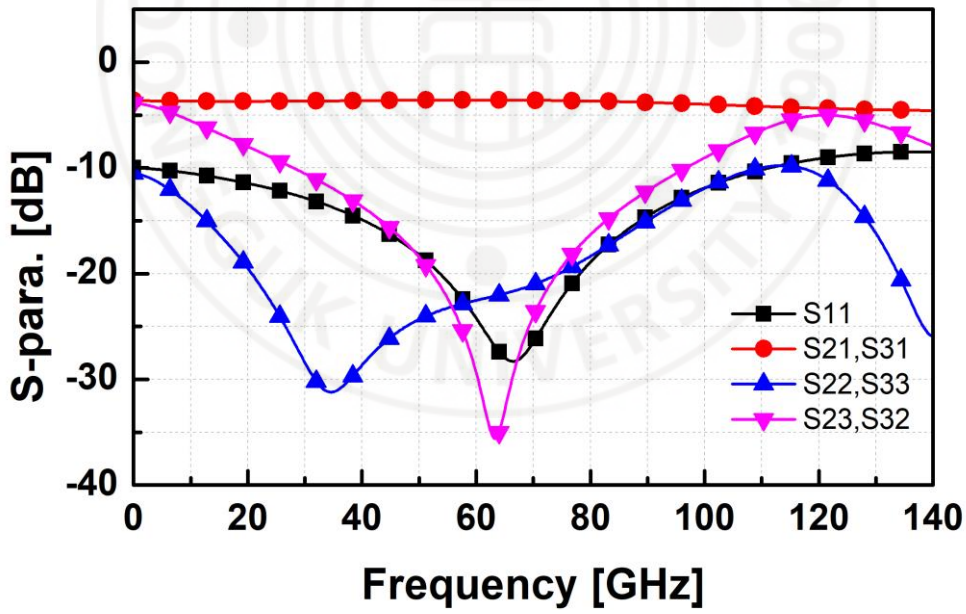


Figure 3.4-5 S-parameter simulation results of designed Wilkinson divider

3.4.2 Flip-chip transition modeling

For the transition between the MZM substrate and DA substrate, the Flip-chip bonding has been considered. Due to its stable electrical interconnections, low cost, and high reliability, flip-chip transition has become a promising alternative to bond-wire in microwave and millimeter wave frequency. In high-speed communication and switching devices, flip-chip bonding offers the advantage of short interconnects, which reduces inductance. Also improves packing density and total package size can be reduced [18]. Signals can be routed directly into the core of the die, rather than needing to be redirected to the edges, since the entire surface of the die can be interconnected. Flip-chip transitions may cause performance degradation at higher frequencies due to parasitic effects. To achieve good transitions from dc to millimeter wave frequencies, flip-chip bonding structure should be taken into consideration.

To consider the transition between the Mach-Zehnder optical modulator substrate and the drive amplifier substrate, the s4p file obtained through simulation after modeling in HFSS was used. In Figure 3.4-6 3D-EM model of Flip-chip transition based on HFSS is shown. Microstrip-based transmission lines with characteristic impedance 50 Ohm were connected to the pad of the drive amplifier board, and coplanar waveguide-based transmission lines with characteristic impedance 50 Ohm were connected to the pad of the MZM.

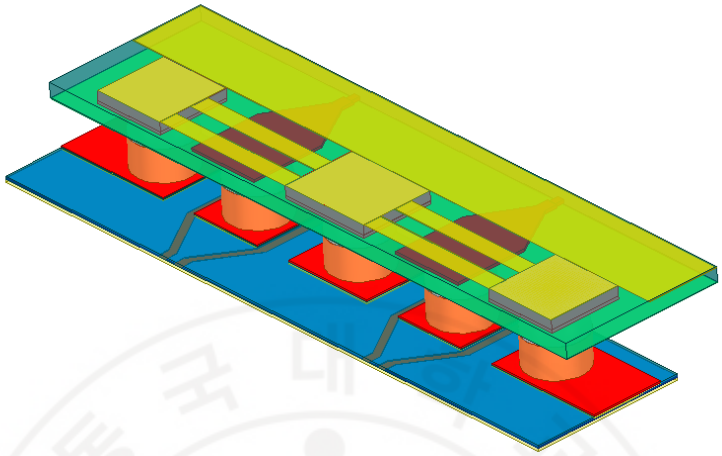


Figure 3.4-6 3D-EM model of Flip-chip transition based on HFSS

It was necessary to analyze whether the effects of flip-chip conversion had no problem with the operation of the driver and MZM. Figure 3.4-7 shows the equivalent circuit of flip-chip transition structure. It is found that the series resistance R_S and shunt conductance G'_M, G'_D are small and can be neglected. The effective bump impedance $Z_b = \sqrt{L_S/(C_M + C_D)}$ [19] should be close enough to the system impedance 50 Ohm to avoid deteriorating RF performance. The series inductance is found to be 140.4 pH and the shunt capacitance $(C_M + C_D)$ is 114.4 fF at 70 GHz which is extracted from HFSS EM simulation. So, the effective bump impedance can be calculated as 35 Ohm. The effective capacitance which is given by $C_{eff} = (C_M + C_D) - \left(L_S/{Z_0}^2\right)$ [20] and can be calculated by 58.2 fF. Even though effective bump impedance is 35 Ohm and flip-chip transition shows an capacitive property with solder and copper pillar, as mentioned in Chapter 3.1.1, frequency response is

still affordable and it is shown in S-parameter and Eye diagram simulations at following Chapters.

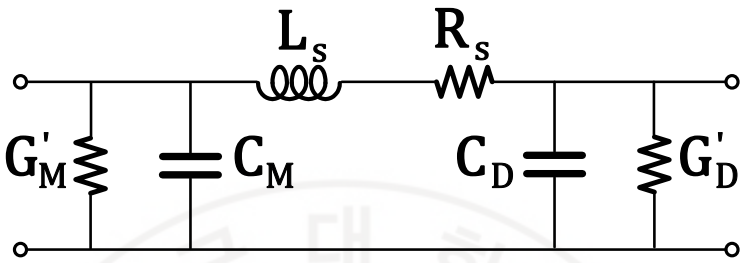


Figure 3.4-7 Equivalent circuit of flip-chip transition

The simulated S-parameters of the designed flip-chip transition model are shown in Figure 3.4-8. The insertion loss of the flip-chip transition is 0.32dB at 50GHz and 0.54dB at 70GHz.

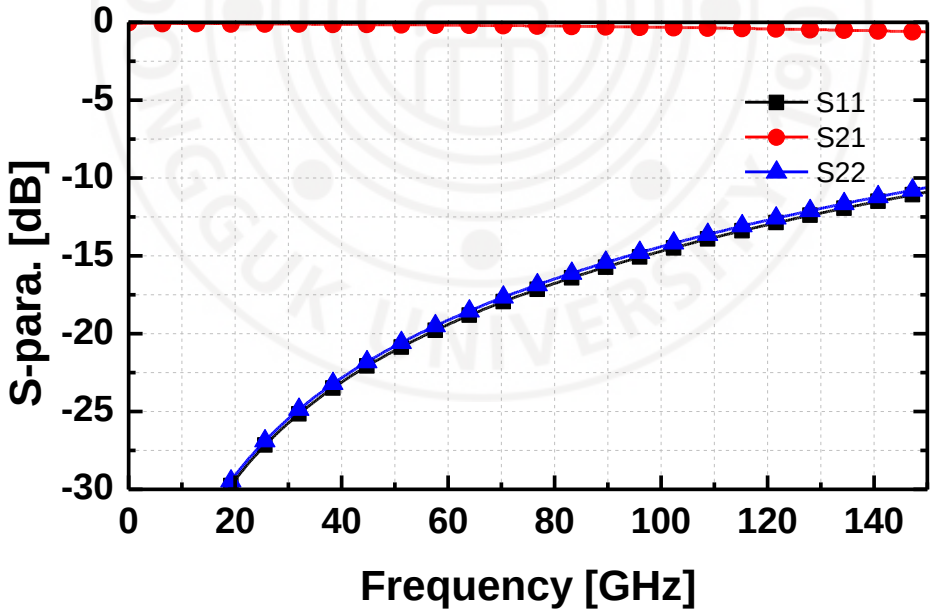


Figure 3.4-8 S-parameter simulation results of flip-chip transition model

3.4.3 Microstrip based delay line design

The delay line was designed to have the appropriate delay time instead of a linear structure so the electrical signal can be synchronized with the optical signal on a limited chip area using a microstrip line with 50 Ohm characteristic impedance. Figure 3.4-9 and 3.4-10 show the layout of designed delay line and 3D-EM model of designed delay line based on HFSS respectively. The simulated S-parameters of the designed delay line are shown in Figure 3.4-11. The insertion loss of the delay line is 2.3 dB at 50 GHz and 2.7 dB at 70 GHz. Because of this inevitable loss from delay line, DA1 is designed with seven stages while DA2 is designed with eight stages to compensate the delay line attenuation.

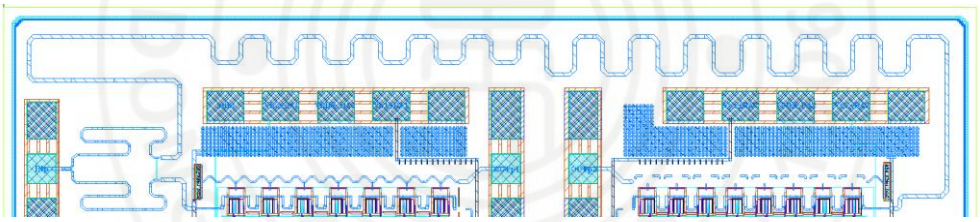


Figure 3.4-9 Layout of designed delay line

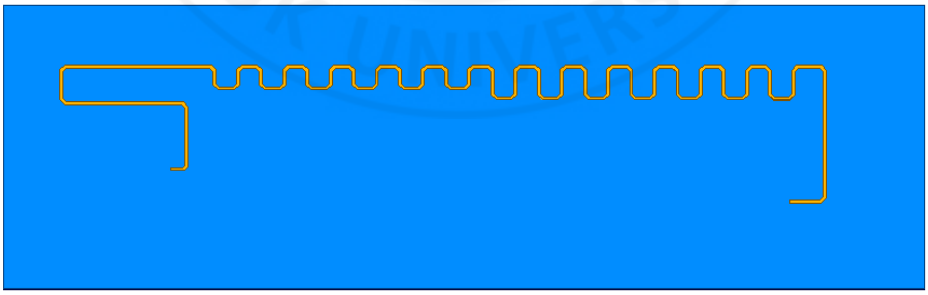


Figure 3.4-10 3D-EM model of designed delay line based on HFSS

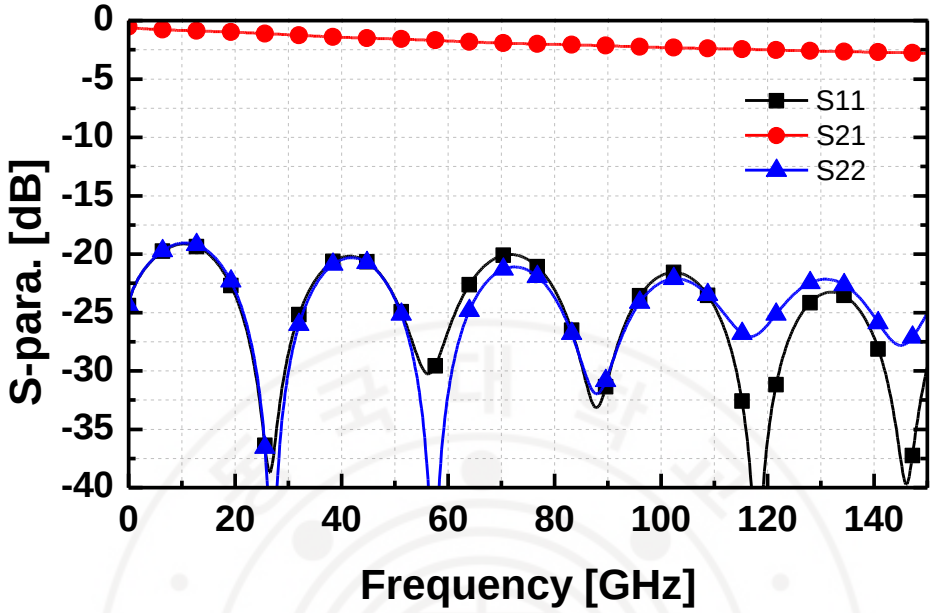


Figure 3.4-11 S-parameter simulation results of designed delay line

3.5 Full chip Layout and Simulation results

With the designed components of driver in Chapter 3 and designed standalone DA introduced in Chapter 2, full chip layout and simulation results of whole structure including DA1(7stage), DA2(8stage), Wilkinson divider, flip-chip transition and delay line is introduced in this Chapter 3.5. In all simulations, the junction in the structure of dual driving driver 1 and driver 2 with a single differential input is included. Figure 3.5-1 shows the full chip Layout of propose ultra-wideband driver. Bypass capacitors are placed around DC pads and Metal 2 ground plane is used to make all the TOP Metal transmission line has 50 Ohm characteristic impedance. Scanchain which controls the tuning network is placed at DA1 part and output bit line is connected to each MOSFET switches and decoder with buffers.

The effect of tuning network is shown in this Chapter. Power consumption of the designed driver was 2.86W, and the chip size was 2.76 mm^2. All the biases are applied through the pad. The drain bias 1.2V is used for scanchain operation. The collector bias for the DA1 and DA2 was 6.3V and 6.8V respectively. For the base bias of the common emitter amplifier (Q2) of cascode unit cell was 1.1V and common base amplifier (Q1) of cascode unit cell was 2.5V.

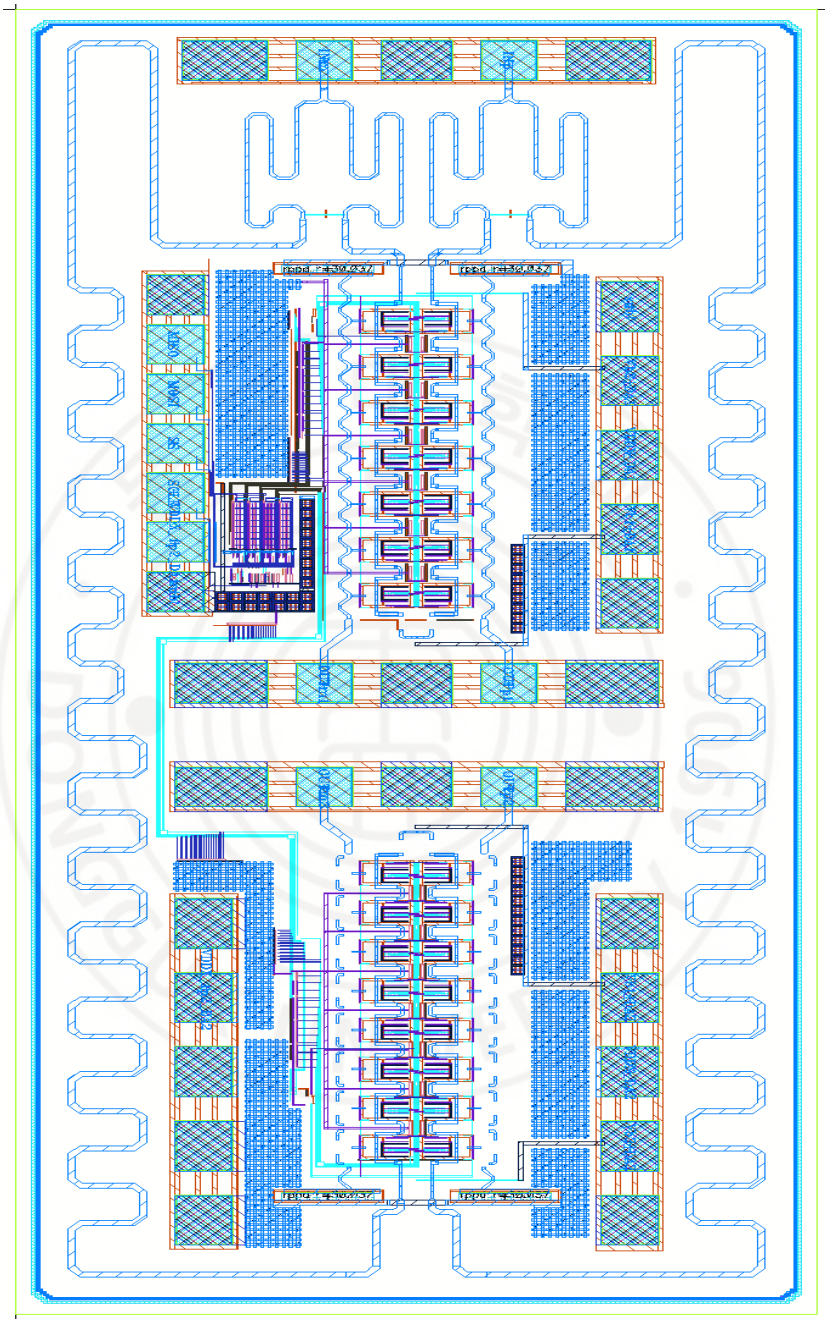
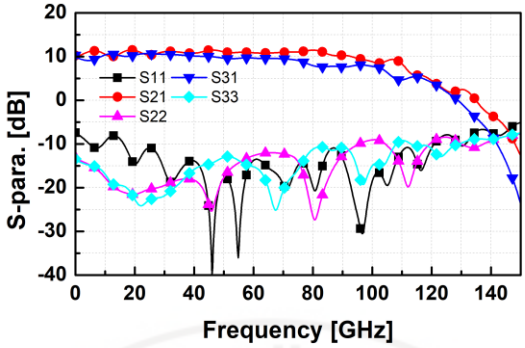


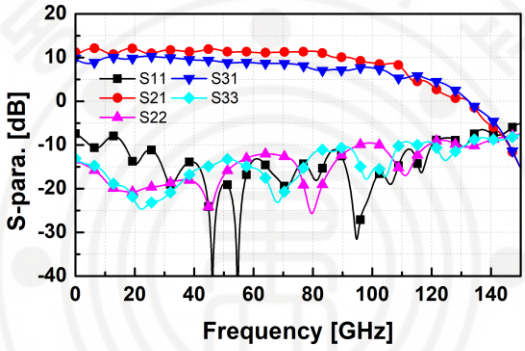
Figure 3.5-1 Full chip layout of proposed ultra-wideband driver

3.5.1 Small signal simulation results

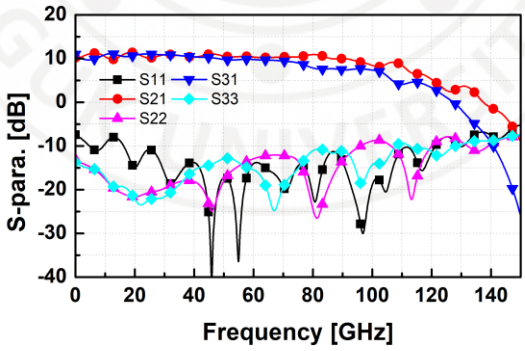
The simulated S-parameters of the designed driver (DA1, DA2) are shown in Figure 3.5-2. Figure 3.5-2 (a) shows the result under C bank ctrl bit : 11111 / R bank ctrl voltage 0.8 V condition for DA1, under C bank ctrl bit : 11111 / R bank ctrl voltage 1.3 V condition for DA2. The designed driver (DA1, DA2) achieves 3-dB gain bandwidth of 105 GHz (100 kHz-105 GHz) with a peak gain of 11.4 dB and 11.1 dB respectively. Within the 3-dB gain bandwidth, input and output return losses are greater than 5 dB. In result of figure 3.5-2 (b) and (c), the effect of proposed tuning network. For figure 3.5-2 (b) the condition of tuning network is C bank ctrl bit : 11111 / R bank ctrl voltage 2.5 V for DA1, C bank ctrl bit : 00000 / R bank ctrl voltage 0.3 V for DA2. And for figure 3.5-2 (c) the condition of tuning network is C bank ctrl bit : 00000 / R bank ctrl voltage 0.3 V for DA1, C bank ctrl bit : 11111 / R bank ctrl voltage 2.5 V for DA2. Both DA1 and DA2 achieved a 3dB gain bandwidth of 100 kHz-105 GHz. Within the 3dB gain bandwidth, the peak gain is 11.4 dB for DA1 and 11.1 dB for DA2. Because of the Wilkinson divider for the dual driving with single input operation, compare to standalone DA simulation result the gain was around 3.5 dB decreased. With the result of figure 3.5-2 (b) and (c), we can confirm that the function of the tuning network operates by comparing the condition of tuning network (b - gain of DA1 is maximized, gain of DA2 is minimized) and the condition of tuning network (c - gain of DA1 is minimized, gain of DA2 is maximized).



(a) **DA1 : C bank ctrl bit : 11111 / R bank ctrl voltage : 0.8V**
DA2 : C bank ctrl bit : 11111 / R bank ctrl voltage : 1.3V



(b) **DA1 : C bank ctrl bit : 11111 / R bank ctrl voltage : 2.5V**
DA2 : C bank ctrl bit : 00000 / R bank ctrl voltage : 0.3V



(c) **DA1 : C bank ctrl bit : 00000 / R bank ctrl voltage : 0.3V**
DA2 : C bank ctrl bit : 11111 / R bank ctrl voltage : 2.5V

Figure 3.5-2 Simulated S-parameters of proposed driver (DA1, DA2)

3.5.2 Eye diagram and transient simulation results

In chapter 3.5.2, the differential signal's waveform of eye diagram or time domain transient simulation results are presented at the point marked with a red arrow (DA1, MZM1 path) and blue arrow (DA2, MZM2 path). Figure 3.5-3 shows the block diagram of separated two signal paths to check the amplified PAM-4 signals by DA.

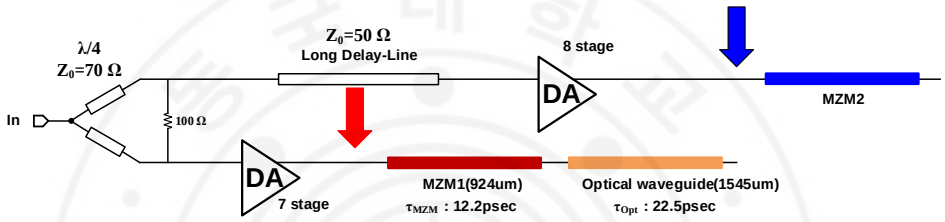
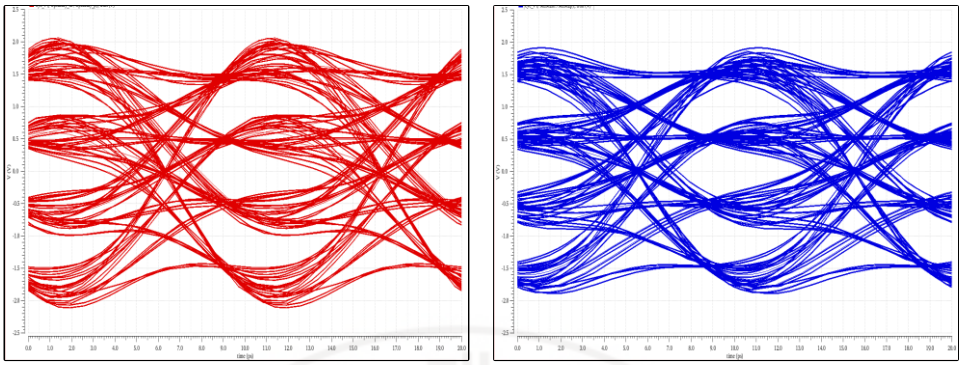
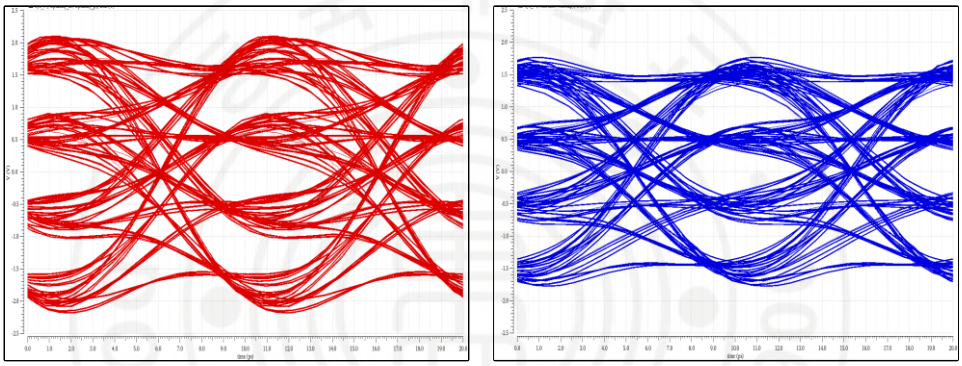


Figure 3.5-3 Block diagram of separated two signal paths

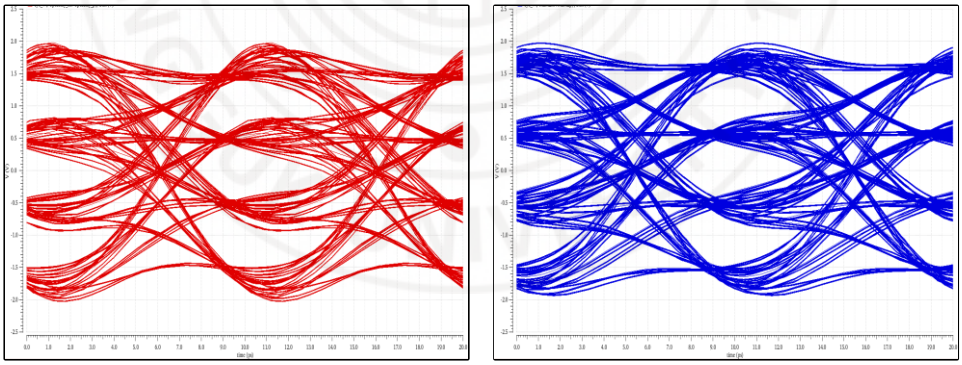
Figure 3.5-4 shows eye diagram of two electrical signals at each path in three different condition same as small signal simulation results. When a 1 Vppd PAM-4 signal of 100GBaud (200Gb/s) was input to the proposed driver, 3 eye openings are clear and the output voltage magnitude of the DA1, DA2 reach 3 Vppd, and the Eye linearity and Eye skew in the output signal's eye diagram were 1 and 0, respectively. Also, we can check the effect of tuning network with the amplitude of each eye diagram as we have already checked that the gain is controlled with condition of C bank control bit and R bank control voltage.



(a) **DA1 : C bank ctrl bit : 11111 / R bank ctrl voltage : 0.8V** **DA2 : C bank ctrl bit : 11111 / R bank ctrl voltage : 1.3V**



(b) **DA1 : C bank ctrl bit : 11111 / R bank ctrl voltage : 2.5V** **DA2 : C bank ctrl bit : 00000 / R bank ctrl voltage : 0.3V**



(c) **DA1 : C bank ctrl bit : 00000 / R bank ctrl voltage : 0.3V** **DA2 : C bank ctrl bit : 11111 / R bank ctrl voltage : 2.5V**

Figure 3.5-4 Eye diagram of separated two signal paths

As mentioned in Chapter 4.3, in the proposed system, synchronization between the electrical signal passing through DA2 with delay line and the optical signal passing through DA1, MZM1, and optical waveguide is key point. Figure 3.5-5 shows the block diagram of separated two signal's paths. The red arrow points out the signal that passed DA1, MZM1, and optical waveguide and the blue arrow points out the signal that passed delay line and DA2. Figure 3.5-6 shows the time domain transient simulation result of Path 1 and Path 2.

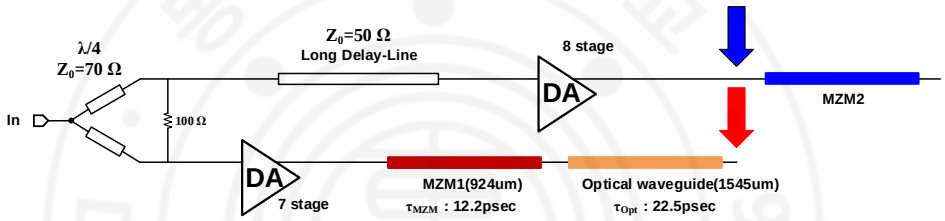
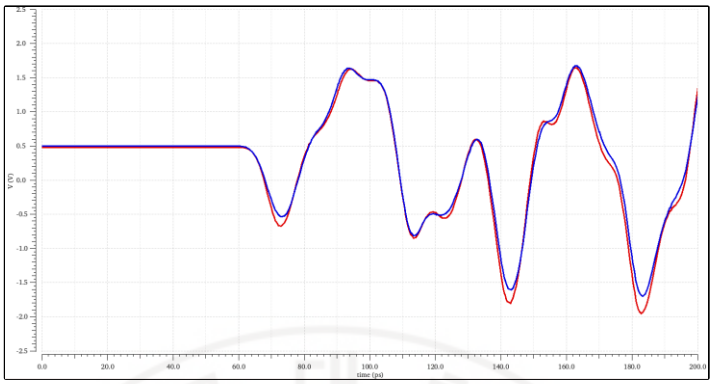
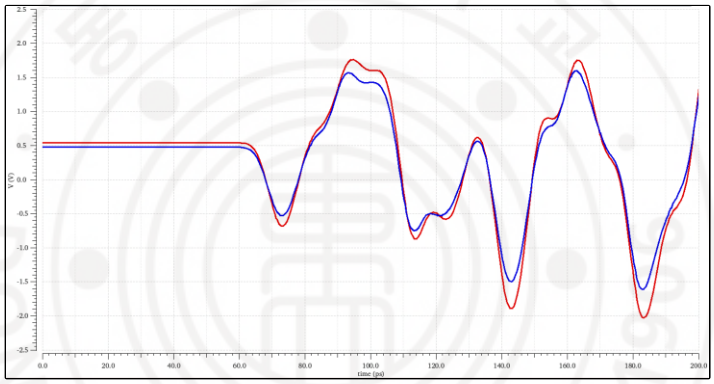


Figure 3.5-5 Block diagram of separated two signal paths

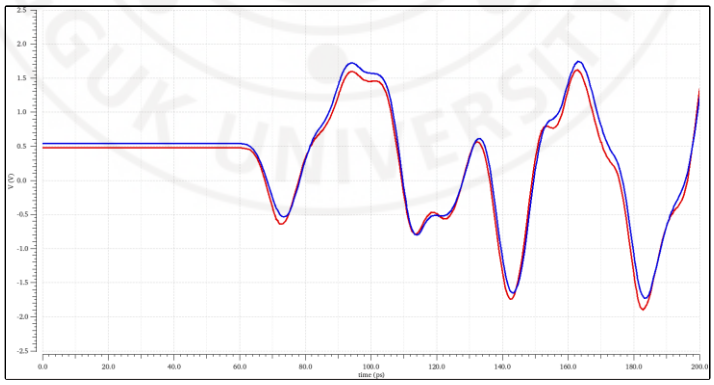
The signal at each point is well matched in time domain with the estimated 34.7psec delay of MZM1 and optical waveguide. The synchronization between the electrical signal input to MZM2's electrode and the optical signal passing through MZM1 and the optical waveguide was checked.



(a) **DA1 : C bank ctrl bit : 11111 / R bank ctrl voltage : 0.8V**
DA2 : C bank ctrl bit : 11111 / R bank ctrl voltage : 1.3V



(b) **DA1 : C bank ctrl bit : 11111 / R bank ctrl voltage : 2.5V**
DA2 : C bank ctrl bit : 00000 / R bank ctrl voltage : 0.3V



(c) **DA1 : C bank ctrl bit : 00000 / R bank ctrl voltage : 0.3V**
DA2 : C bank ctrl bit : 11111 / R bank ctrl voltage : 2.5V

Figure 3.5-6 Time domain transient simulation result of two paths

3.6 Measurement set up

This measurement plan covers the measurement of small signal and large signal characteristics for a single driver. The SPI scan-chain pads and bias pads are bonded to the PCB, and RF input and output are measured using probes. In order to the differential structure design, measurement using a balun is required. However, the measurement set up with balun has difficulties in achieving accurate calibration. The measurement will be proceeded by using a GSG probe with one port of the differential structure is open. Also, DA1 and DA2 measurements should be proceeded separately due to the difficulty of physically probing the two output RF pads. It's possible because high isolation is achieved with the Wilkinson divider.

Vector network analyzer (VNA) can be used to measure S-parameters. Figure 3.6-1 and 3.6-2 show the small signal gain measurement setup for DA1 DC-40GHz and 67GHz-110GHz, respectively. The VNA N5224A available to operate from 10MHz to 43.5GHz, so measurements for the 67GHz-110GHz band will be taken using the W-band extender. Figure 3.6-3 and 3.6-4 show the setup for large-signal measurements. For the large signal measurement, signal generator Agilent 83623B can be used to generate input power at each frequency and and the output power is measured using a power meter. The Agilent 83623B available to generate input power from 10MHz to 20GHz, so measurements for the 70GHz-110GHz will be taken using the x6 frequency multiplier. In addition, measurements for the 43.5GHz to 75GHz band can be possible using the V-band VCO and power meter.

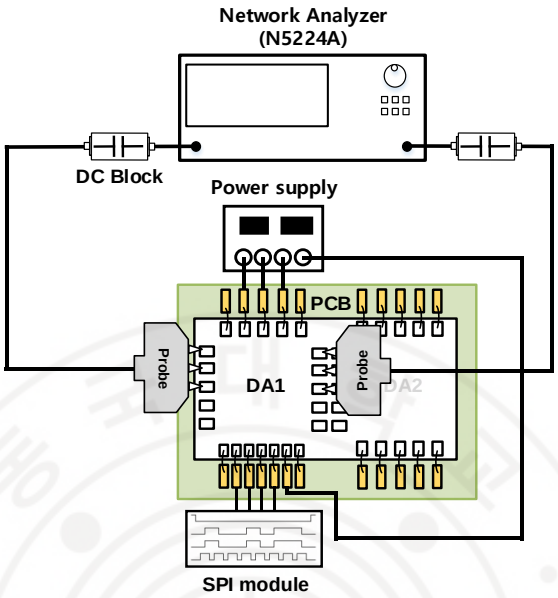


Figure 3.6-1. Small signal measurement for 10MHz-40GHz

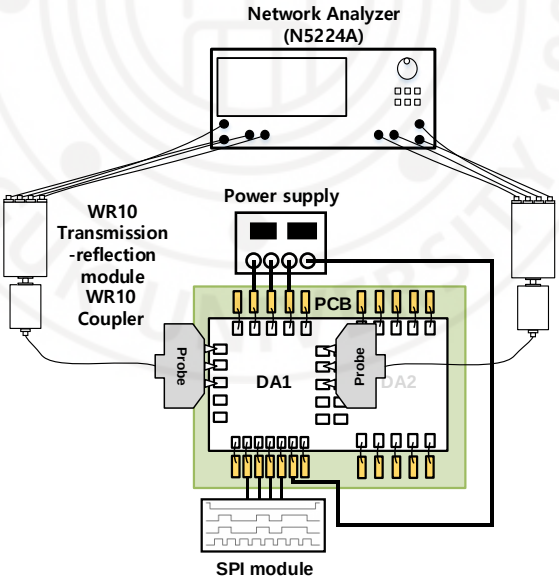


Figure 3.6-2 Small signal measurement for 67-110GHz

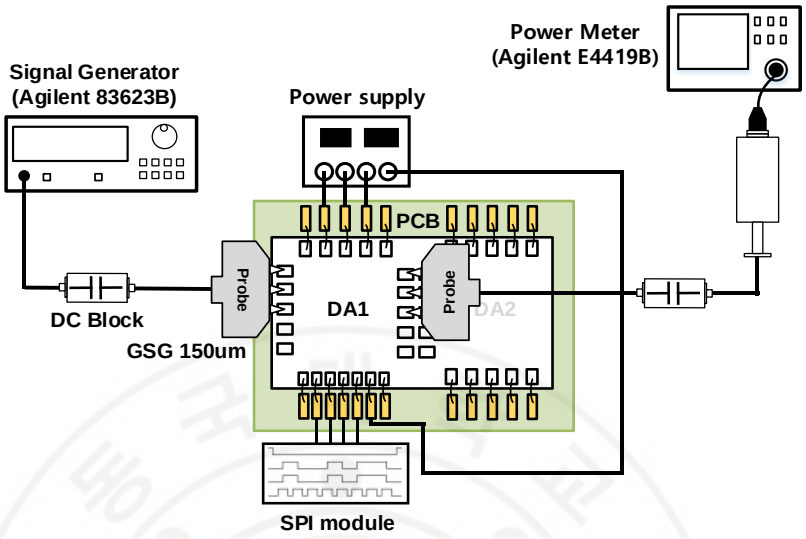


Figure 3.6-3. Large signal setup for 10MHz-20GHz

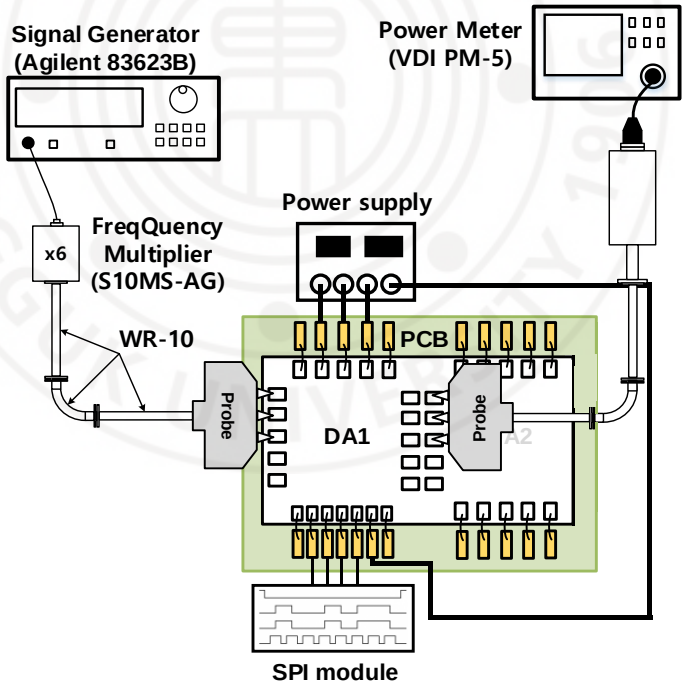


Figure 3.6-4 Large signal setup for 70-110GHz

Chapter 4 Conclusion

This thesis demonstrated ultra-wideband driver using IHP 130nm SiGe BiCMOS technology for optical communication systems with MZM. Two distributed amplifiers (DA), a Wilkinson divider, and a delay line for electrical and optical signal synchronization were designed on single chip for dual driving operation with single input. The designed driver achieved a 3dB gain bandwidth of 100 kHz-105 GHz with a peak gain of over 11 dB. When a 100GBaud PAM-4 signal was input at 1 Vppd, the output voltage magnitude of the driver reached 3 Vppd with high fidelity. The synchronization between the electrical signal input to MZM2's electrode and the optical signal passing through MZM1 and optical waveguide was also realized. Proposed ultra-wideband driver can be implemented in a high-speed optical communication systems which has advantage of low power consumption and minimal loss over long distances.

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국문 초록

본 학위 논문은 PAM-4(4 Level Pulse Amplitude Modulation)를 적용한 200Gb/s급 마하젠더 광변조기(Mach-Zehnder Modulator, MZM)용 구동기의 구현에 관한 것이다. 차세대 초고속 광네트워크 구현을 목적으로 제안된 구동기는 2개의 초광대역 분산형 증폭기(Distributed Amplifier, DA)와 Wilkinson 분배기, 그리고 변조용 전기 신호와 광신호의 동기화를 위한 지연기로 구성되어있다. Degenerated Cascode 단위 셀을 적용한 분산형 증폭기는 왜곡을 최소화하면서 200Gb/s급 PAM-4신호를 Segmented-MZM 전극에 구동하기 위해서 가변형 RC 네트워크를 Emitter degeneration에 적용하여 Eye Diagram의 충실도를 개선하고자 하였다. 해당 RC 네트워크는 SPI 스캔 체인(Serial Peripheral Interface Scan-chain)을 통해 출력 비트가 MOS 스위치의 게이트에 연결되어 유효 커패시턴스, 저항값을 제어하도록 설계되었다.

설계된 구동기의 DA1은 7단, DA2는 8단으로 구성하여 지연기에서 발생하는 삽입손실이 DA2를 통해 보상될 수 있도록 구현하였다. 설계된 구동기는 100 kHz - 105 GHz의 3dB 이득대역폭과 70 GHz 대역에서 9 dB 이상의 소신호 이득, 70GHz에서 출력 포화전력 18 dBm를 달성하였다. 설

계된 구동기의 소모전력은 2.86W이며 칩의 크기는 2.76 mm^2 이다. 설계된 구동기에 100GBaud의 PAM-4신호를 1Vppd로 입력하였을 때, 구동기의 양 출력 전압 크기는 3Vppd를 만족하였으며, 출력 신호의 Eye Diagram에서 Eye linearity는 1, Eye skew는 0을 달성하였으며 본 구동기와 연결된 MZM1과 광도파로를 통과한 광신호가 MZM2의 전극에 입력되는 전기신호와 잘 동기화됨을 확인하였다.